ESC-TR-97-145

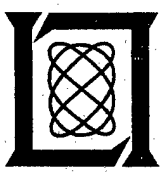
23 Feb 99

Quarterly Technical Report

Solid State Research

1998:3

Lincoln Laboratory
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LEXINGTON, MASSACHUSETTS



Prepared for the Department of the Air Force under Contract F19628-95-C-0002.

This report is based on studies performed at Lincoln Laboratory, a center for research operated by Massachusetts Institute of Technology. The work was sponsored by the Department of the Air Force under Contract F19628-95-C-0002.

The ESC Public Affairs Office has reviewed this report, and it is releasable to the National Technical Information Service, where it will be available to the general public, including foreign nationals.

This technical report has been reviewed and is approved for publication.

FOR THE COMMANDER

Gary Tutungian
Administrative Contracting Officer
Contracted Support Management

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

SOLID STATE RESEARCH

QUARTERLY TECHNICAL REPORT

1 MAY – 31 JULY 1998

ISSUED 23 FEBRUARY 1999

LEXINGTON MASSACHUSETTS

ABSTRACT

This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 May through 31 July 1998. The topics covered are Quantum Electronics, Electro-optical Materials and Devices, Submicrometer Technology, High Speed Electronics, Microelectronics, Analog Device Technology, and Advanced Silicon Technology. Funding is provided by several DoD organizations—including the Air Force, Army, BMDO, DARPA, Navy, NSA, and OSD—and also by the DOE, NASA, and NIST.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

INTRODUCTION

1. QUANTUM ELECTRONICS

Passively Q-switched Nd:YAG microchip lasers have been developed that produce up to 250 μJ per pulse at 1.064 μm, with a pulse duration of 380 ps. The infrared output has been harmonically converted to 532, 355, and 266 nm with high efficiency.

2. ELECTRO-OPTICAL MATERIALS AND DEVICES

Bromine ion-beam-assisted etching has produced smooth vertical sidewalls in GaAs, GaP, InP, AlSb, and GaSb as well as in the usual alloys formed from these materials. Our etching experience and the vapor pressure data for bromine with group III and group V elements has led us to believe that all of the various technologically important III-V binaries, ternaries, and quaternaries can be etched with this technology.

The in-plane Seebeck coefficient, Hall coefficient, and electrical resistivity of PbTe/Te superlattice structures grown by molecular beam epitaxy have been measured at 300 K. The results have shown that a significant enhancement of the in-plane Seebeck coefficient, thermoelectric power factor, and figure of merit has been achieved.

High-performance InAsSb/AlAsSb double heterostructures for mid-infrared, optically pumped lasers have been grown by molecular beam epitaxy. At ~80 K, a record optical-to-optical power conversion efficiency of 9.5% has been obtained for ~1-W long-pulse, 3.85-μm emission with 1.9-μm pumping.

Novel techniques for the accurate alignment and attachment of mass-transported microlenses to the facets of diode lasers, including tapered lasers and tapered laser arrays, have been demonstrated. Techniques for the alignment of a single element tapered laser, a GaP microlens, and a single-mode optical fiber in a compact package have also been demonstrated with an optical coupling efficiency of 60% at 980 nm.

3. SUBMICROMETER TECHNOLOGY

Line-edge roughness has been investigated experimentally for silylated top-surface imaging resist. The observed roughness has been shown to be a function of the aerial image quality and thus may limit the allowable defocus margin for the process.

Microbridge materials optimized for room-temperature infrared microbolometers have been fabricated using plasma-enhanced chemical vapor deposition. The films deposited from tetramethyldisiloxane are compatible with current CMOS processing and have been shown to have adequate thermal conductivity, infrared absorption, and mechanical strength for use as microbolometer membranes.

4. HIGH SPEED ELECTRONICS

Two-port small-signal S-parameter measurements have been performed on the first source-up 6H-SiC and drain-up 4H-SiC vertical field-effect transistors (VFETs). The 12-GHz unity current gain frequency and 4-GHz maximum frequency of oscillation obtained for the 4H-SiC VFET are the highest values obtained for any vertical transistor fabricated in SiC to date, demonstrating the potential of this technology for this material system.

5. MICROELECTRONICS

Resistive-gate charge-coupled device (CCD) technology is being reexamined as a high-yield process for some large-area CCD applications. Preliminary results on two candidate films, lightly doped polysilicon and cermet, have shown promise in meeting the requirements for the resistive gates.

6. ANALOG DEVICE TECHNOLOGY

A 1.1% bandwidth 3-pole transmit filter based on stripline-like circular resonators, made using thin film superconductors, has been built and tested. The filter frequency response is independent of power up to at least 72 W, the maximum power available to us, and the intermodulation products for two 20-W input tones in-band is at least 104 dBc.

7. ADVANCED SILICON TECHNOLOGY

A study has been undertaken to assess possible hardware implementations of a new signal compression algorithm, targeted at the compression of data from infrared atmospheric sensors aboard a NASA earth observation satellite. One of the options, which offers potential advantages over the alternatives, is an application-specific integrated circuit that could be built in Lincoln Laboratory's fully depleted 0.25-μm silicon-on-insulator CMOS process.

REPORTS ON SOLID STATE RESEARCH

1 MAY THROUGH 31 JULY 1998

PUBLICATIONS

High-Precision Film Thickness Determination Using a Laser-Based Ultrasonic Technique	M. J. Banet* M. Fuchs* J. A. Rogers* J. H. Reinold, Jr. J. M. Knecht M. Rothschild R. Logan* A. A. Maznev* K. A. Nelson*	*Appl. Phys. Lett.* **73**, 169 (1998)
A 1.3-GHz SOI CMOS Test Chip for Low-Power High-Speed Pulse Processing	R. Berger W. G. Lyons A. M. Soares	*IEEE J. Solid-State Circuits* **33**, 1259 (1998)
Calculated and Measured Transmittance of Metallodielectric Photonic Crystals Incorporating Flat Metal Elements	A. Kao K. A. McIntosh O. B. McMahon R. Atkins S. Verghese	*Appl. Phys. Lett.* **73**, 145 (1998)
Effects of the Internal Loss on Power Efficiency of Mid-Infrared InAs–GaInSb–AlSb Quantum-Well Lasers and Comparison with InAsSb Lasers	H. Q. Le C. H. Lin* S. J. Murray* R. Q. Yang* S. S. Pei*	*IEEE J. Quantum. Electron.* **34**, 1016 (1998)

*Author not at Lincoln Laboratory.

Damage Testing of Pellicles for 193-nm Lithography	V. Liberman R. R. Kunz M. Rothschild J. H. C. Sedlacek R. S. Uttaro A. Grenville* A. K. Bates* C. Van Peski*	*Proc. SPIE* **3334**, 480 (1998)
Assessment of Optical Coatings for 193-nm Lithography	V. Liberman M. Rothschild J. H. C. Sedlacek R. S. Uttaro A. Grenville* A. K. Bates* C. Van Peski*	*Proc. SPIE* **3334**, 470 (1998)
Thin Silicide Development for Fully-Depleted SOI CMOS Technology	H. I. Liu J. A. Burns C. L. Keast P. W. Wyatt	*IEEE Trans. Electron Devices* **45**, 1099 (1998)
Metrology Methods for the Quantification of Edge-Roughness	C. M. Nelson S. C. Palmateer T. Lyszczarz	*Proc. SPIE* **3332**, 19 (1998)
Line Edge Roughness in Sub-0.18-μm Resist Patterns	S. C. Palmateer S. G. Cann J. E. Curtin S. P. Doran L. M. Eriksen A. R. Forte R. R. Kunz T. M. Lyszczarz M. B. Stern C. Nelson*	*Proc. SPIE* **3333**, 634 (1998)

*Author not at Lincoln Laboratory.

Screening of Excitons in GaN Crystals	D. C. Reynolds* D. C. Look* B. Jogai* R. J. Molnar	*J. Phys.* **10**, 5577 (1998)
Photolithography at Wavelengths Below 200 nm	M. Rothschild	*Proc. SPIE* **3274**, 222 (1998)
Pattern Transfer for Diffractive and Refractive Microoptics	M. B. Stern	*Microelectron. Eng.* **34**, 299 (1997)
Phase Noise of a Resonant-Tunneling Relaxation Oscillator	S. Verghese C. D. Parker E. R. Brown	*Appl. Phys. Lett.* **72**, 2550 (1998)

ACCEPTED FOR PUBLICATION

Bromine Ion-Beam-Assisted Etching of InP and GaAs	W. D. Goodhue D. E. Mull J. M. Rossler Y. Royter C. G. Fonstad*	*J. Vac. Sci. Technol.*
Modeling the Microwave Impedance of High-T_c Long Josephson Junctions	D. E. Oates C. J. Lehner* Y. M. Habib* G. Dresselhaus* M. Dresselhaus*	*J. Superconduct.*

*Author not at Lincoln Laboratory.

PRESENTATIONS†

Photolithography at Wavelengths Below 200 nm	M. Rothschild	1998 Conference on Lasers and Electro-Optics, San Francisco, California, 3-8 May 1998
The Photomixer Transceiver	S. Verghese K. A. McIntosh	
Optical Lithography at Feature Sizes of 0.25 μm and Below	R. R. Kunz	Lincoln Laboratory Technical Seminar Series, University of California, Berkeley, California, 8 May 1998
Microwave Superconducting Devices and Material Nonlinearity	D. E. Oates	Technical Seminar, Texas Center for Superconductivity, University of Houston, Houston, Texas, 8 May 1998
Critical Issues for Projection Lithography at 157 nm	T. M. Bloomstein M. Rothschild M. W. Horn R. B. Goodman D. E. Hardy	42nd International Conference on Electron, Ion and Photon Beam and Nanofabrication, Chicago, Illinois, 26-29 May 1998
Near-Field Optical Lithography at 193 nm	M. W. Horn M. Rothschild R. B. Goodman	
Line Edge Roughness: Measurements, Mechanisms and Impact on Future Lithographies	S. C. Palmateer R. R. Kunz T. M. Lyszczarz M. B. Stern	

†Titles of presentations are listed for information only. No copies are available for distribution.

In-Situ Monitoring of GaSb, GaInAsSb and AlGaAsSb	C. J. Vineis C. A. Wang K. F. Jensen*	9th International Conference on Metal Organic Vapor Phase Epitaxy, La Jolla, California, 30 May–4 June 1998
Recent Progress in GaInAsSb Thermophotovoltaics Grown by Organometallic Vapor-Phase Epitaxy	C. A. Wang D. C. Oakley H. K. Choi G. W. Charache*	
OMVPE Growth and Characterization of GaInAsSb for Thermophotovoltaics	C. A. Wang	16th Conference on Crystal Growth and Epitaxy, Fallen Leaf Lake, California, 7-10 June 1998
A GaN-Based Avalanche Photodiode	S. Verghese K. A. McIntosh R. J. Molnar C. L. Chen K. M. Molvar R. L. Aggarwal I. Melngailis	56th Annual Device Research Conference, Charlottesville, Virginia, 22-24 June 1998
Flux, Penetration, Pinning and Nonlinearities	D. E. Oates	High Temperature Superconductors in High Frequency Fields, Stockholm, Sweden, 22-25 June 1998
Bromine Ion-Beam-Assisted Etching of III-V Semiconductors	W. D. Goodhue D. E. Mull S. S. Choi Y. Royter C. G. Fonstad*	40th Electronic Materials Conference, Charlottesville, Virginia, 24-26 June 1998
Preparation and Characterization of New and Novel Pb Chalcogenide-Based MBE-Grown Superlattice Structures with Enhanced Thermoelectric Figures of Merit	T. C. Harman D. L. Spears M. P. Walsh	

*Author not at Lincoln Laboratory.

Optical Lithography Below 100 nm	R. R. Kunz	Microfabrication, Nanostructured Materials and Biotechnology Conference, Tegernsee, Germany, 28 June–3 July 1998
MIT Lincoln Laboratory's 0.25 μm, Low Power, High Performance, Fully Depleted SOI CMOS Technology	C. L. Keast	Semicon West '98, San Francisco, California, 13 July 1998
Testing of Optical Materials for 193-nm Lithographic Applications	V. Liberman M. Rothschild J. H. C. Sedlacek R. S. Uttaro A. Grenville A. K. Bates C. Van Peski	SPIE International Symposium on Optical Science, Engineering and Instrumentation, San Diego, California, 19-24 July 1998
Investigation of Three-Dimensional Metallodielectric Photonic Crystals Incorporating Flat Metal Elements	K. A. McIntosh S. Verghese R. G. Atkins	

ORGANIZATION

SOLID STATE DIVISION

D. C. Shaver, *Head*
R. W. Ralston, *Associate Head*
N. L. DeMeo, Jr., *Assistant*

Z. L. Lemnios, *Senior Staff*

J. W. Caunt, *Assistant Staff*
K. J. Challberg, *Administrative Staff*
J. D. Pendergast, *Administrative Staff*

SUBMICROMETER TECHNOLOGY

M. Rothschild, *Leader*
T. M. Lyszczarz, *Assistant Leader*
T. H. Fedynyshyn, *Senior Staff*
R. R. Kunz, *Senior Staff*

Astolfi, D. K.
Bloomstein, T. M.
Cohen, A. E.*
Craig, D. M.
DiNatale, W. F.
Doran, S. P.
Efremow, N. N., Jr.
Forte, A. R.
Geis, M. W.
Goodman, R. B.
Krohn, K. E.
Liberman, V.
Maki, P. A.
Palmacci, S. T.
Palmateer, S. C.
Sedlacek, J. H. C.
Stern, M. B.
Uttaro, R. S.

QUANTUM ELECTRONICS

A. Sanchez-Rubio, *Leader*
T. Y. Fan, *Assistant Leader*
T. H. Jeys, *Senior Staff*

Aggarwal, R. L.
Buchter, S.
Cook, C. C.
Daneu, J. L.
Daneu, V.
DiCecca, S.
Dill, C., III
Le, H. Q.
Ochoa, J. R.
Zayhowski, J. J.

ELECTRO-OPTICAL MATERIALS AND DEVICES

D. L. Spears, *Leader*
J. C. Twichell, *Assistant Leader*
H. K. Choi, *Senior Staff*
R. C. Williamson, *Senior Staff*

Bailey, R. J.
Betts, G. E.
Choi, S. S.*
Connors, M. K.
Cronin, S.*
Donnelly, J. P.
Goodhue, W. D.
Harman, T. C.
Liau, Z. L.
Manfra, M. J.
Missaggia, L. J.
Mull, D. E.
Napoleone, A.
Nee, P.*
Nitishin, P. M.
Oakley, D. C.
O'Donnell, F. J.
Poillucci, R. J.
Reeder, R. E.
Taylor, P. J.
Turner, G. W.
Vineis, C. J.*
Walpole, J. N.
Wang, C. A.
Wasserman, J.

*Research Assistant

HIGH SPEED ELECTRONICS

M. A. Hollis, *Leader*
E. R. Brown, *Assistant Leader*†

Bozler, C. O.
Calawa, A. R.‡
Calawa, S. D.
Chen, C. L.
Graves, C. A.
Harris, C. T.
Lightfoot, A.
Mahoney, L. J.
Mathews, R. H.
McIntosh, K. A.
Molnar, R. J.
Parameswaran, L.
Rabe, S.
Rathman, D. D.
Rider, T. H.
Verghese, S.
Young, A. M.

ANALOG DEVICE TECHNOLOGY

T. C. L. G. Sollner, *Leader*
L. M. Johnson, *Assistant Leader*
A. C. Anderson, *Senior Staff*

Ala'ilima, T. F.
Arsenault, D. R.
Berggren, K. K.
Boisvert, R. R.
Feld, D. A.
Fitch, G. L.
Holtham, J. H.
Lyons, W. G.
Macedo, E. M., Jr.
Murphy, P. G.
Oates, D. E.
Paul, S. A.
Sage, J. P.
Santiago, D. D.
Seaver, M. M.
Slattery, R. L.
Whittington, R. H.

MICROELECTRONICS

B. B. Kosicki, *Leader*
R. K. Reich, *Assistant Leader*
B. E. Burke, *Senior Staff*

Aull, B. F.
Cooper, M. J.
Daniels, P. J.
Doherty, C. L., Jr.
Dolat, V. S.
Donahue, T. C.
Felton, B. J.
Gregory, J. A.
Johnson, K. F.
Lind, T. A.
Loomis, A. H.
McGonagle, W. H.
O'Mara, D. M.
Percival, K. A.
Young, D. J.

ADVANCED SILICON TECHNOLOGY

C. L. Keast, *Leader*
P. W. Wyatt, *Associate Leader*

Berger, R.
Burns, J. A.
Chen, C. K.
Davis, P. V.
D'Onofrio, R. P.
Frankel, R. S.
Fritze, M.
Knecht, J. M.
Newcomb, K. L.
Reinold, J. H., Jr.
Sexton, S. V.
Soares, A. M.
Suntharalingam, V.
Tyrrell, B. M.
Yost, D.-R.
Young, G. R.

‡Part Time
†Intergovernmental Personnel Act assignment

1. QUANTUM ELECTRONICS

1.1 MID- AND HIGH-POWER PASSIVELY *Q*-SWITCHED MICROCHIP LASERS

Passively *Q*-switched microchip lasers are simple, compact, robust sources of short-pulse laser radiation with high peak power and nearly ideal mode quality. Although there are some reports on high-power devices (pumped with 10–12 W of diode power) [1]–[3], most of the work on passively *Q*-switched microchip lasers has concentrated on lasers pumped with ~1 W of diode power [3]–[6]. Here, we give a detailed description of several mid- and high-power lasers in a series of devices recently developed at Lincoln Laboratory. These passively *Q*-switched microchip lasers were designed to be pumped with the output of 3- and 10-W high-power fiber-coupled 808-nm diode-laser arrays. The most powerful of these lasers produces 250 μJ/pulse at 1.064 μm, with a pulse duration of 380 ps and peak power in excess of 570 kW. The infrared output of these devices has been harmonically converted to 532, 355, and 266 nm with high efficiency.

The devices reported here were built and tested for several different applications. There was no attempt to ensure that test conditions on different devices were equivalent, or that the same tests were performed on each device. For example, the pulse energies and thresholds of the lasers are dependent on the magnification of an intermediate lens. Optimization for high energy at low repetition rates requires different focusing than optimization for high repetition rates. Some applications required high-repetition-rate operation, others did not. Each of the lasers was optimized for a particular program under different operating conditions. Nonetheless, the results reported here give a good idea of the capabilities of the technology discussed.

The 3-W-pumped mid-power microchip lasers discussed here (MPMCL-1, MPMCL-2, and MPMCL-3) all comprise a piece of Nd:YAG diffusion bonded to a 3-mm-long piece of Cr^{4+}:YAG. For MPMCL-1 and MPMCL-2, the Nd:YAG is 3 mm long. For MPMCL-3, the Nd:YAG has a length of 9 mm. The Nd:YAG in all of the devices is doped at 1.1 wt% Nd; the Cr^{4+}:YAG has an unsaturated absorption of 1.5 cm^{-1} at 1.064 μm. In addition to these two materials, devices MPMCL-2 and MPMCL-3 have a piece of undoped YAG diffusion bonded to the Cr^{4+}:YAG on the face opposite the Nd:YAG, as shown in Figure 1-1. The dimensions of the crystals are given in Table 1-1. Dielectric coatings are applied directly on the crystals. The input coating, deposited on the Nd:YAG, is antireflecting at the pump wavelength (808 nm) and highly reflecting (>99.9%) at the oscillating frequency. The output coating on all of the devices has a reflectivity of 60% at the oscillating frequency (1.064 μm).

The undoped YAG in MPMCL-2 and MPMCL-3 is used to lengthen the cavity in a way that maintains the robustness of the device. The increased cavity length results in a larger oscillating-mode diameter and, therefore, more efficient use of the pump. In addition, it leads to a longer pulse length, which can be advantageous for pumping optical parametric oscillators [1]. The Cr^{4+}:YAG is kept near the center of the cavity so that spatial hole burning in the saturable absorber has the largest possible effect on maintaining single-longitudinal-mode operation of the laser. The faces of the composite Nd:YAG/Cr^{4+}:YAG/undoped-YAG material system are polished flat, to a parallelism of better than 10 μrad.

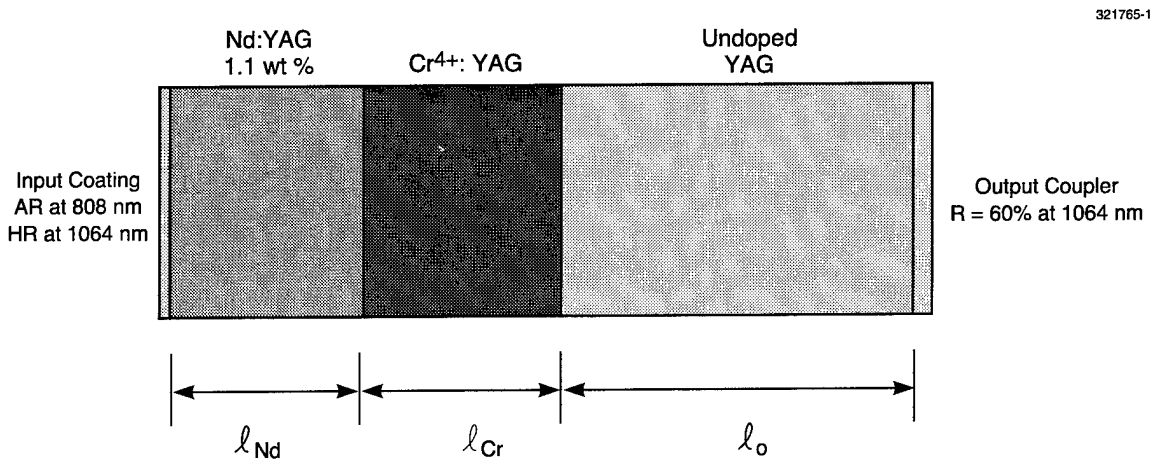


Figure 1-1. Schematic of 3-W-pumped mid-power passively Q-switched microchip lasers.

TABLE 1-1
3-W-Pumped Mid-Power Passively Q-Switched Microchip Laser Parameters

Device	Nd:YAG ℓ_{Nd} (mm)	Cr^{4+}:YAG ℓ_{Cr} (mm)	Output YAG Cap ℓ_O (mm)	Cr^{4+}:YAG Absorption α (cm^{-1})	Output Coupler R (%)
MPMCL-1	3	3	0	1.5	60
MPMCL-2	3	3	6	1.5	60
MPMCL-3	9	3	12	1.5	60

The microchip lasers are cut to a nominal 2 × 2-mm cross section and bonded to a gold-coated oxygen-free-copper heatsink with thermally conductive epoxy (Thermalbond 4951, from Thermalloy, Inc.). Before bonding, the bonded sides of the lasers were ground flat for good thermal contact. The opposite sides were polished to a window-like finish so that the epoxy bond could be observed through the YAG. The surfaces to be bonded were meticulously cleaned to ensure the minimal bond thickness and avoid the formation of bubbles in the epoxy. A small amount of epoxy was applied to the heatsink. The laser was placed on the epoxy and carefully aligned before being clamped in place. The epoxy was then cured at 50°C for 1 h. Typical epoxy thicknesses are 5 μm.

To pump the mid-power microchip lasers, the 3-W output of a fiber-coupled diode-laser array (Model OPC-D003-808-HB/100 3-W cw high-brightness fiber-coupled diode laser, from Opto Power, Inc.) was passed through a protective window and imaged into the gain medium (Nd:YAG) with a commercially available, antireflection-coated, matched pair of aspheric lenses (Model C220MP-B fiber-to-fiber high-numerical-aperture (NA) matched pair, NA = 0.25, f = 11 mm, from Thorlabs, Inc.). The positions of the fiber end, lens, and microchip laser were empirically optimized, but typically resulted in a unity magnification of the fiber facet (core diameter = 100 μm, NA = 0.2) in the Nd:YAG. The protective window was coated to be antireflecting at the pump wavelength and highly reflective at both the lasing wavelength and its second harmonic. This prevented any high-peak-power laser radiation (and its second harmonic) from being coupled into the fiber, propagating back to the pump diodes, and causing damage. The protective window was also used to hermetically seal the microchip laser head, even when the pump diodes were disconnected. All of the elements of the mid-power microchip laser head, with the exception of the three O-rings used to seal the protective window to the mounting block (bottom heatsink), the laser cover to the mounting block, and the output window to the laser cover, are shown in Figure 1-2. Mounted passively Q-switched mid-power microchip lasers are shown in Figure 1-3. A completely packaged device is shown in Figure 1-4.

The repetition rate of the passively Q-switched lasers is controlled by pulsing the pump diodes. The length of the diode ON pulse is set to allow exactly one output pulse from the microchip laser for each pulse of the diodes. MPMCL-1 and MPMCL-2 can be pulse pumped with 3 W of optical power. At low pulse repetition rates, MPMCL-1 produces 30 μJ/pulse with a 700-ps pulse duration. MPMCL-2 produces 40 μJ/pulse with a 1200-ps pulse duration. MPMCL-1 can also be cw pumped, to produce 330 mW of infrared output at 16-kHz repetition rate. MPMCL-2 cannot be cw pumped. With 3 W of pump power, it has a maximum pulse repetition rate of ~3 kHz, limited by thermal effects in the YAG crystals. MPMCL-3 requires more than 3 W to reach threshold. With 5 W of pump power (from a particularly "hot" Model OPC-D003-808-HB/100 3-W diode laser) it can be pulsed at up to 2.5 kHz and produces 65-μJ pulses of 2200-ps duration. The performance of the mid-power passively Q-switched microchip lasers is summarized in Table 1-2 for a pulse repetition rate of 500 Hz.

With the use of 3 (or 5) W of pump power, all of the mid-power devices operate in a linearly polarized, single longitudinal mode, with diffraction-limited output. When pulse pumped, the amplitudes and pulse widths are stable to within 1%. When MPMCL-1 is cw pumped, its output bifurcates at pulse repetition rates above 15 kHz. Alternating pulses are in different longitudinal and polarization modes, each with slightly different amplitude.

The mid-power microchip lasers were also pumped with 10 W of diode power (Model OPC-D010-808-HB/250 10-W cw high-brightness fiber-coupled diode laser, from Opto Power, Inc.), producing ~3 times more energy per pulse than when pumped with 3 W. Similar devices, pumped with 12 W, have been previously reported [1]–[3]. The performance with 10-W pumping at a pulse repetition rate of 500 Hz is included in Table 1-2. When pumped with 10 W, none of the mid-power devices maintained single-mode performance at pulse repetition rates much above 2 kHz. Multimode oscillation is often followed by damage to the output facet of the laser.

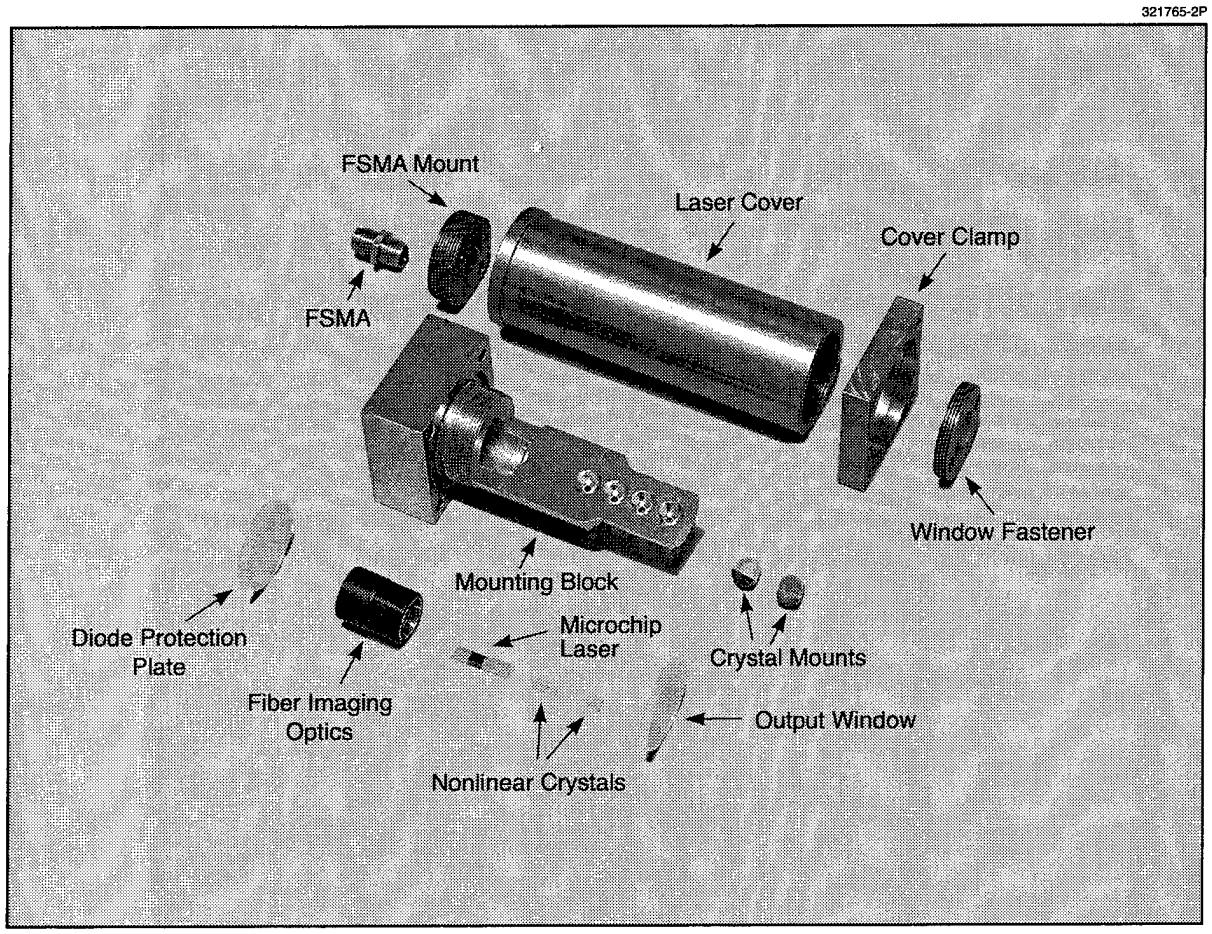


Figure 1-2. Components of mid- and high-power passively Q-switched microchip laser head.

The four 10-W-pumped high-power infrared microchip lasers discussed here (HPMCL-1, HPMCL-2, HPMCL-3, and HPMCL-4) comprise a four-crystal sandwich of undoped YAG, Nd:YAG, Cr^{4+}:YAG, and undoped YAG, diffusion bonded to each other in that order, as shown in Figure 1-5. The Nd:YAG in all of the devices is doped at 1.1 wt% Nd. HPMCL-2 uses a piece of Cr^{4+}:YAG with an unsaturated absorption of 1.5 cm^{-1} at 1.064 μm. For the rest of the devices, the unsaturated absorption of the Cr^{4+}:YAG is 6 cm^{-1} at 1.064 μm. The dimensions of the crystals are given in Table 1-3. Devices HPMCL-1 and HPMCL-2 have an unsaturated round-trip loss due to the saturable absorber of 83%. The unsaturated round-trip loss in HPMCL-3 and HPMCL-4 is 93%. Dielectric coatings are applied to the undoped YAG endcaps. For all devices, the input-side coating is antireflecting at the pump wavelength and

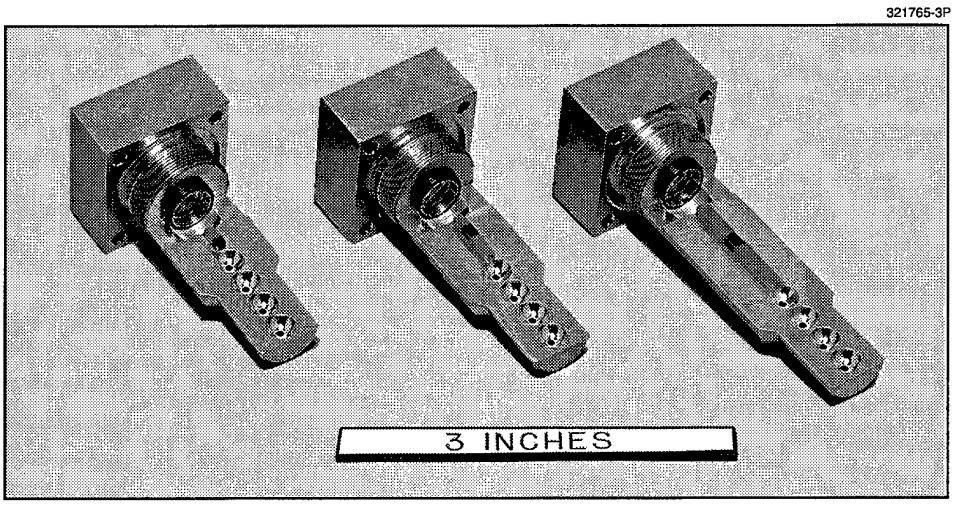


Figure 1-3. Mounted mid-power passively Q-switched microchip lasers.

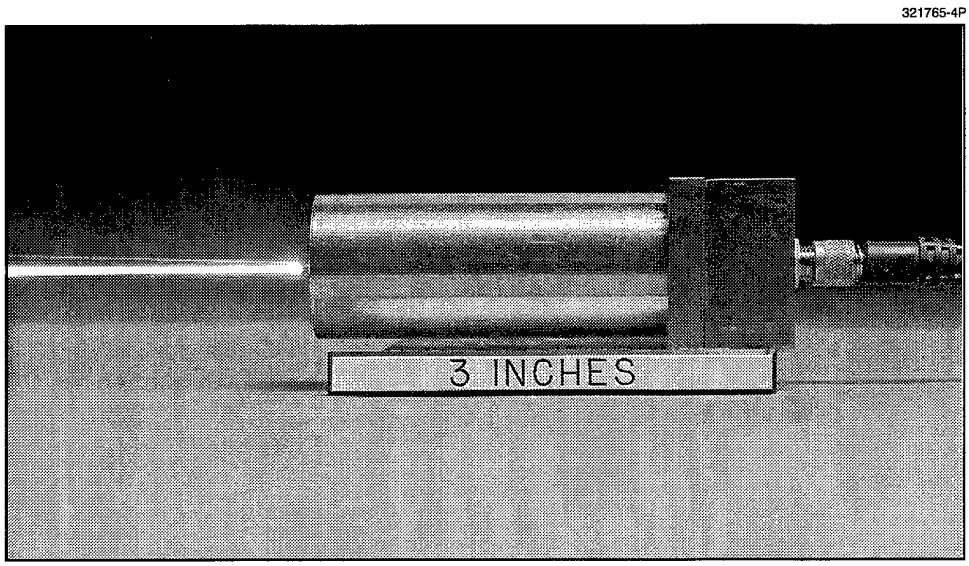


Figure 1-4. UV passively Q-switched microchip laser head.

TABLE 1-2
Mid-Power Device Characteristics at 500 Hz

Device	Pump Power (W)	Pulse Energy (μJ)	Pulse Width (ps)	Beam Waist (μm)	Peak Power (kW)	Peak Intensity (GW/cm^2)	Peak Fluence (J/cm^2)
MPMCL-1	3	30	700	60	37	0.65	0.53
MPMCL-2	3	40	1200	70	29	0.37	0.52
MPMCL-3	5	65	2200	85	25	0.22	0.57
MPMCL-1	10	100	650	85	132	1.16	0.88
MPMCL-2	10	150	1000	100	129	0.82	0.95
MPMCL-3	10	180	2000	120	77	0.34	0.80

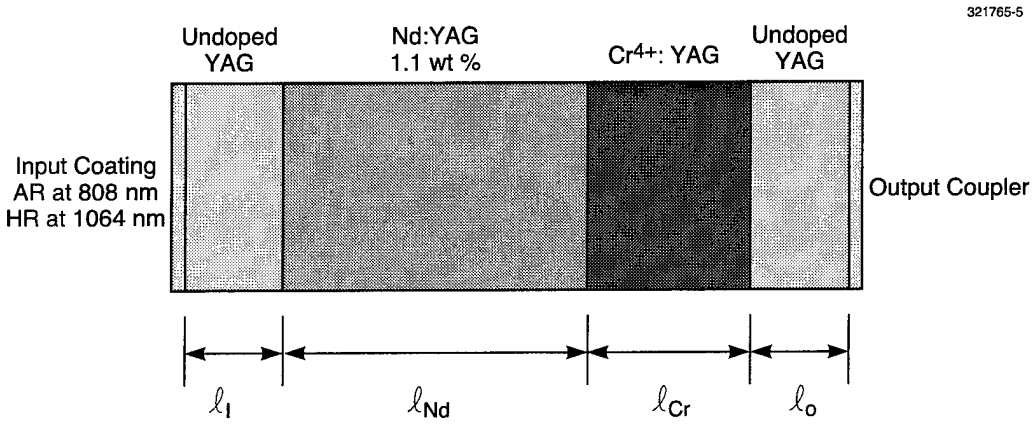


Figure 1-5. Schematic of 10-W-pumped high-power passively Q-switched microchip lasers.

TABLE 1-3
10-W-Pumped High-Power Passively Q-Switched Microchip Laser Parameters

Device	Nd:YAG ℓ_{Nd} (mm)	Nd:YAG ℓ_{Nd} (mm)	Cr^{4+}:YAG ℓ_{Cr} (mm)	Output YAG Cap ℓ_O (mm)	Cr^{4+}:YAG Absorption α (cm^{-1})	Output Coupler R (%)
HPMCL-1	1	3	1.5	1	6	40
HPMCL-2	1	4	6	1	1.5	40
HPMCL-3	1	3	2.25	1	6	26
HPMCL-4	1	4	2.25	3	6	26

highly reflecting (>99.9%) at the oscillating frequency. The output coatings of HPMCL-1 and HPMCL-2 have a reflectivity of 40% at 1.064 μm. The reflectivity of the output coatings for HPMCL-3 and HPMCL-4 is 26%.

The undoped YAG endcaps are used to improve the damage threshold of the devices. The use of undoped endcaps has become common practice in high-power lasers. Since there is no absorption of pump or laser radiation in the undoped materials, thermal stress at the YAG/dielectric-coating and dielectric-coating/air interfaces is reduced. This improves the damage threshold of the coatings. It has also been observed that, independent of thermal stress, undoped materials have a higher damage threshold than doped material, and the damage usually occurs at the surface of the materials. Diffusion bonding buries the Nd:YAG and Cr^{4+}:YAG ends, protecting them from damage.

The faces of the composite undoped-YAG/Nd:YAG/Cr^{4+}:YAG/undoped-YAG material system are polished to a parallelism of better than 10 μrad. The surface is polished so that there are no apparent scratches, sleeks, or digs in the active region when viewed with a Nomarski microscope at magnifications up to 800×. This level of surface finish was used to avoid the high fields that can arise at surface irregularities and nucleate damage. (The intensity of the infrared beam exiting the laser is as high as 10 GW/cm^2; we were concerned about field-induced damage.) The surfaces were meticulously cleaned before applying high-damage-threshold dielectric coatings. The output coatings were finished with a half-wave layer of SiO_2 to improve the damage threshold and robustness of the devices. Having taken the precautions described in this paragraph, we have not observed coating damage to any of the high-power devices over a cumulative operating time of several hundred hours.

The high-power microchip lasers are cut to a nominal 2 × 2-mm cross section and bonded to a gold-coated oxygen-free-copper heatsink with thermally conductive epoxy in the same way as the mid-power lasers. For high-repetition-rate operation of the 10-W-pumped devices, it was necessary to

heatsink the lasers from the top as well as the bottom. A U-shaped piece of oxygen-free copper was carefully machined to contact the top of the laser and the bottom heatsink on both sides of the laser, within a tolerance of 5 μm. The length of the heatsink was equal to the length of the laser. Thermal epoxy was applied to the three contact areas, the top heatsink was clamped in place, and the epoxy was cured. Contact to the sides of the laser was avoided. The top heatsink was added in a separate step, not at the same time the laser was attached to the bottom heatsink. This facilitated alignment of the laser and made it easier to optimize the primary thermal contact between the laser and the bottom heatsink. The laser was tested, and the alignment checked, at low repetition rates before the top heatsink was added. Thermal contact to both the top and bottom of the laser results in symmetry in the thermal loading of the devices and prevents thermal destabilization of the microchip cavity. We noticed, however, that at high duty cycles the polarization axis of the laser can switch from being defined by internal properties of the YAG crystals to being oriented with the thermal stress induced by the heatsink geometry. This problem can be avoided by pretesting and properly aligning the microchip lasers before they are diced into 2 × 2-mm devices.

To pump the high-power microchip lasers, the 10-W output of a fiber-coupled diode laser array was passed through a protective window and imaged into the gain medium (Nd:YAG) with a commercially available, antireflection-coated, matched pair of aspheric lenses. The positions of the fiber end, lens, and microchip laser were empirically optimized, but typically resulted in a ~0.5× magnification of the fiber facet (core diameter = 250 μm, NA = 0.2) in the Nd:YAG. All of the elements of the high-power microchip laser heads, with the exception of the laser itself and the top heatsink described above, are the same as for the mid-power devices, and are shown in Figure 1-2; the completed high-power device is identical in appearance to the laser shown in Figure 1-4.

For HPMCL-1 to reach threshold with a 10-W pump requires a diode ON pulse of only 140 μs, a duration well below the spontaneous lifetime of the upper laser level. This device can be pumped with as little as 6.5 W from the 10-W diode-laser array and produces 130-μJ pulses with 390-ps pulse width at low repetition rates. A high-brightness 3-W diode-laser array has also been used to pump HPMCL-1. When pumped with 3 W, the beam cross section and the output power of the laser are reduced by about a factor of 2. HPMCL-2 requires a 300-μs ON pulse with 10-W pumping and produces 225-μJ pulses with 700-ps duration. This pump pulse duration is greater than the spontaneous lifetime of the upper laser level. HPMCL-3 and HPMCL-4 required, respectively, pump powers of 11 and 15 W (from a particularly hot Model OPC-D010-808-HB/250 10-W diode laser) to reach threshold. They produce 200 μJ in a 310-ps pulse, and 250 μJ in a 380-ps pulse, respectively. The performance of the high-power passively Q-switched microchip lasers, at 500-Hz pulse repetition rate, is summarized in Table 1-4.

Although Table 1-4 only contains data for a pulse repetition rate of 500 Hz, HPMCL-1 can be pumped at frequencies up to 5.5 kHz (with 10-W pumping). At high pulse repetition rates the radius of the beam waist decreases to ~60 μm, owing to increased thermal mode guiding. The pulse energy decreases to 110 μJ/pulse and the pulse width remains about the same. HPMCL-1 can also be cw pumped to generate ~650 mW of 1.064-μm output. HPMCL-2 operates at repetition rates up to 2 kHz. The beam waist at 2 kHz decreases to 60 μm, without a significant change in its output energy or pulse width. HPMCL-2 cannot be cw pumped. HPMCL-3 and HPMCL-4 have not been tested at pulse repetition rates above 500 Hz.

TABLE 1-4
High-Power Device Characteristics at 500 Hz

Device	Pump Power (W)	Pulse Energy (μJ)	Pulse Width (ps)	Beam Waist (μm)	Peak Power (kW)	Peak Intensity (GW/cm^2)	Peak Fluence (J/cm^2)
HPMCL-1	3	70	400	55	150	3.2	1.5
HPMCL-1	10	130	390	70	286	3.7	1.7
HPMCL-2	10	225	700	90	276	2.2	1.8
HPMCL-3	11	200	310	60	554	9.8	3.5
HPMCL-4	15	250	380	60	565	10.0	4.4

All of the high-power devices operate in a linearly polarized, single longitudinal mode, with diffraction-limited output. When pulse pumped, the amplitudes and pulse widths are stable to within 1%. When HPMCL-1 is cw pumped, its output bifurcates. Alternating pulses are in different longitudinal and polarization modes, each with slightly different amplitude.

As shown in Table 1-4, the peak powers of the high-power microchip lasers are several hundred kW, and the output intensities are several GW/cm^2. Peak fluences are several J/cm^2. These intensities and fluences are the reason for the care that was taken in the surface preparation and coating of the laser facets.

The output of several of the microchip lasers described above was harmonically converted into the visible and uv. To frequency double the infrared output of the microchip lasers we use low-temperature hydrothermally grown KTP, oriented for Type II phase matching (obtained from SYNOPTICS, a division of Litton Airtron). The KTP crystals were cut with an orientation of $\theta = 90°$ and $\phi = 27°$. Proper phase matching is achieved for $\theta = 90°$ and $\phi = 24.3°$. Phase matching therefore occurs when the crystal faces are tilted ~4.5° (27° – 24.3° multiplied by an index of 1.7 for KTP) with respect to the infrared output of the microchip laser. This "misorientation" ensures that the KTP does not reflect light directly back into the laser and that multiply reflected beams inside the KTP do not overlap to generate an interference pattern in its output. (SYNOPTICS preferred to misorient the KTP rather than wedge its surfaces.) The input face of the KTP was coated to be antireflecting at 1.064 μm and highly reflecting at 532 nm. The high reflector at 532 nm is used to help protect the pump diodes from any backreflected green light that might otherwise couple into the pump fiber and damage the pump diodes. The output of the KTP is antireflecting at both 1.064 μm and 532 nm.

The damage threshold for KTP is ~1 GW/cm^2. This is above the output intensity of the mid-power microchip lasers. For the mid-power devices, the KTP was positioned next to the output facet of the laser.

The peak output intensity of the high-power microchip lasers, however, is much greater than the damage threshold of KTP. For this reason, for the high-power devices we mount the KTP so that its input facet is >1.5 cm from the output facet of the microchip laser, where diffraction reduces the peak intensities to below the threshold for bulk material damage in the KTP. Gray tracking (laser-induced photorefractive damage) can still be a problem. We observe gray tracking in flux-grown materials and high-temperature hydrothermally grown materials at much lower intensities. We have not seen gray tracking in low-temperature hydrothermal KTP, even at 1 GW/cm^2.

The KTP crystals we use are ~5 mm long with a 2 × 2-mm cross section. They are mounted in a V-shaped groove machined in 1/4-in. stainless-steel ball bearings, seen in Figure 1-2. The V groove is cut so that the center of the KTP sits at the center of the ball bearing. The bottom of the ball bearing (directly opposite the V groove) is drilled and tapped so that an alignment stick can be screwed into it. The ball bearing is mounted in a socket in the microchip laser mounting block so that the center of the KTP is positioned in the output beam of the microchip laser. For each socket in the mounting block, a V slot is cut from the bottom of the mounting block with its apex at the center of the socket hole. In the plane perpendicular to the microchip output, the slot opens a >90° wedge. In the orthogonal direction the slot is 5/32 in. wide. (This is slightly different than shown in Figures 1-2 and 1-3.)

To mount the KTP on the laser mounting block, the KTP is epoxied into the ball bearing. The alignment stick is screwed into the ball bearing and lowered through the socket in the mounting block. A spring is used to hold the ball bearing tightly in the socket as the end of the alignment stick is moved with micrometers to properly phase match the nonlinear interaction. The V groove allows the KTP to be rotated by up to 90° to obtain the proper orientation with respect to the polarization of the microchip laser. (If more than 90° rotation is needed, the nonlinear crystal can be rotated in the ball bearing by 90° increments.) The 5/32-in. slot thickness is sufficient to allow proper alignment in that direction, and the alignment stick can be rotated to obtain proper orientation in the final direction. Alignment is performed actively, with the laser running. When proper alignment is obtained, the top of the ball bearing is epoxied to the mounting block. After the epoxy is cured, the alignment stick is removed.

Typical doubling efficiencies for MPMCL-1 and HPMCL-1, when the KTP is mounted as described above and aligned for maximum doubling efficiency, are about 60%. The performance of these devices, at high pulse repetition rates, is summarized in Table 1-5. Similar efficiencies are obtained for the other devices. The high-intensity output of these lasers is sufficient to effectively saturate the doubling process in KTP.

Third-harmonic, 355-nm uv output is obtained by summing the 1.064-μm fundamental with the second harmonic of the microchip laser output in properly oriented BBO (uv-grade material selected for minimum scattering and intensity-linked absorption, from Cleveland Crystals, Inc.) using Type I phase matching. The crystals are ~5 mm long with a 2 × 2-mm cross section. The input face of the BBO is coated to be antireflecting at both input frequencies. The output is antireflection coated at 355 nm.

TABLE 1-5
Average Power Generated by MPMCL-1 and HPMCL-1 at Fundamental and Harmonics

Device	Maximum Pump Power (W)	Pulse Repetition Rate (kHz)	1064-nm Average Power (mW)	532-nm Average Power (mW)	355-nm Average Power (mW)	266-nm Average Power (mW)
MPMCL-1	3	15	309	186	Not tested	37
HPMCL-1	10	5.5	605	335	104	66

When the KTP used for second-harmonic generation is aligned for maximum second-harmonic efficiency, the 1.064-μm radiation at the most intense positions within the laser pulse (both temporally and spatially) is depleted, resulting in poor third-harmonic generation. To more nearly optimize the third-harmonic generation, we rotate the KTP in the plane normal to the incident infrared beam until the second-harmonic efficiency is reduced to ~67% of its maximum value. This ensures that there are about as many usable infrared photons as green photons exiting the KTP. Furthermore, by rotating the KTP in the proper direction, these infrared photons are mostly polarized parallel to the green photons, so that they can be efficiently used in Type I uv generation [5]. Once the KTP is aligned as described, we mount the BBO in a socket in the mounting block immediately following the one used for the KTP (center-to-center spacing of the sockets is 1/4 in.) and actively align it in a manner similar to that described for the KTP.

Using the procedure described above, we obtain 19 μJ/pulse of 355-nm output at pulse repetition rates up to 5.5 kHz from a nonlinear system built around HPMCL-1. In the near field the output beam has a nearly diffraction-limited "top-hat" profile in the direction of walk-off in the BBO, with a diameter of ~400 μm. In the opposite dimension the uv beam has a nearly diffraction-limited Gaussian profile, with an effective beam waist (the effective beam waist occurs at the output facet of the microchip laser) of ~50-μm radius. The far-field pattern of the output is shown in Figure 1-6.

To obtain fourth-harmonic, 266-nm uv output, we frequency double the 532-nm second harmonic of the microchip laser in properly oriented BBO using Type I phase matching. The crystals are ~5 mm long with a 2 × 2-mm cross section. The input face of the BBO is coated to be antireflecting at 532 nm; the output is antireflection coated at 266 nm.

In the case of fourth-harmonic generation, the KTP used for second-harmonic generation is aligned for maximum second-harmonic efficiency. The BBO is mounted in the next socket, and aligned as previously described. We obtain 12 μJ/pulse of 266-nm output from a nonlinear system built around HPMCL-1, operating at pulse repetition rates up to 5.5 kHz. A nonlinear system built around MPMCL-1 generates

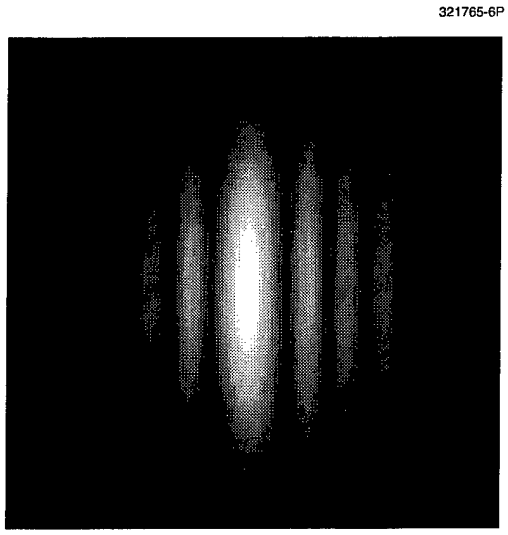


Figure 1-6. Far-field pattern of 355-nm passively Q-switched microchip laser system.

2.5 μJ/pulse at pulse repetition rates up to 15 kHz. The uv performance of these devices is summarized in Table 1-5. In the near field the output beam from both devices has a nearly diffraction-limited top-hat profile in the direction of walk-off in the BBO, with a diameter of ~500 μm. In the opposite dimension the uv beam has a nearly diffraction-limited Gaussian profile, with an effective beam waist of ~50-μm radius. The far-field pattern of the output is qualitatively similar to that shown in Figure 1-6.

KTP is a nearly ideal crystal to use for frequency doubling of the microchip laser output. Very efficient conversion efficiency is obtained at intensities well below the damage threshold. Whether or not KTP is the best crystal to use for frequency doubling as an intermediate step in obtaining the uv harmonics of the high-power passively Q-switched microchip laser is questionable, at least if we insist on using no lenses in the system. Since the uv nonlinear crystal, BBO, must follow the KTP crystal, the optical intensity in the BBO is limited to the intensity in the KTP, even though the damage threshold is an order of magnitude higher for the BBO (10 GW/cm^2 for BBO vs 1 GW/cm^2 for KTP). If we were able to increase the optical intensity in the BBO, we would obtain higher efficiencies in the final step of uv generation. For example, by focusing the output of the KTP into a piece of BBO we have obtained 50% conversion of the input 532-nm radiation to 266 nm. In contrast, the efficiency obtained in the systems described above is ~20%. Given the high output intensities of the high-power microchip lasers, the use of other nonlinear crystals for frequency doubling the 1.064-μm output, such as LBO, may result in higher overall uv efficiency. The lower nonlinear coefficient can be offset by the higher intensities available by putting the crystal closer to the output facet of the laser. (The damage threshold for LBO is 18 GW/cm^2, and gray tracking is not an issue.)

In all of our uv devices, we use only zero-outgas epoxies. It has been our experience that the outgassing from epoxies can be cured by the uv laser radiation, and deposits on the output window of the laser head in the position that the uv radiation passes through the window, destroying the uv beam quality. After all of the nonlinear crystals are mounted, we hermetically seal the laser head in a dry argon environment. A complete, operating uv laser head is shown in Figure 1-4.

We are continuing to push the performance limits of the passively Q-switched microchip lasers. The performance characteristics and reliability of the devices discussed here, particularly MPMCL-1 and HPMCL-1, already make them interesting for a variety of applications. In addition to harmonic conversion, the mid- and high-power microchip lasers can be used to pump parametric devices [1]–[3]. A combination of harmonic and parametric conversion should make it possible to obtain any output wavelength between 5 μm and 200 nm in extremely compact, robust packages. The short pulses are useful for high-precision ranging and imaging. HPMCL-4 is sufficiently powerful to do earth-to-satellite ranging without an amplifier [7]. The high peak powers enable applications in marking, micromachining, laser-induced breakdown spectroscopy (LIBS), matrix-assisted laser desorption and ionization (MALDI), and microsurgery. The focused output of the high-power devices can break down air. The uv output is useful for fluorescence spectroscopy and stereolithography. Additional applications will continue to surface as this technology becomes more readily available.

J. J. Zayhowski C. Dill III
C. Cook J. L. Daneu

REFERENCES

1. J. J. Zayhowski, *IEEE Photon. Technol. Lett.* **9**, 925 (1997).
2. J. J. Zayhowski, *Opt. Lett.* **22**, 169 (1997).
3. J. J. Zayhowski, *Opt. Mater.* **11**, 255 (1999).
4. J. J. Zayhowski, *Laser Focus World* **32**, 73 (1996).
5. J. J. Zayhowski, *Opt. Lett.* **21**, 588 (1996); 1618 (1996).
6. J. J. Zayhowski and C. Dill III, *Opt. Lett.* **19**, 1427 (1994).
7. J. J. Dagnan and J. F. McGarry, *Proc. SPIE* **3218**, 63 (1997).

2. ELECTRO-OPTICAL MATERIALS AND DEVICES

2.1 BROMINE ION-BEAM-ASSISTED ETCHING OF III-V SEMICONDUCTORS

Over the last few years, the group III elements (boron, aluminum, gallium, indium, and thallium) have been combined with the group V elements (nitrogen, phosphorus, arsenic, antimony, and bismuth) to form a number of technologically important semiconductor and semimetal materials. Heterostructures formed from alloys of these III-Vs have been used very successfully to bandgap engineer the materials' properties of many electronic and photonic devices.

The technologically important III-Vs include the binaries GaAs, GaP, GaSb, GaN, InP, InAs, InSb, InN, AlAs, AlP, AlSb, and AlN along with the various ternaries and quaternaries formed from these binaries. Recently III-V compounds with bismuth and thallium have also appeared in the literature. However, in order to fabricate useful devices, suitable etching techniques must be developed.

We have found that bromine ion-beam-assisted etching (Br_2-IBAE) produces smooth vertical sidewalls in GaAs, GaP, InP, AlSb, and GaSb as well as in the usual alloys formed from these materials. However, care must be taken during etching to match the specific material system with an appropriate substrate etch temperature. For example, vertical walls were obtained using substrate temperatures in the range 150–200°C with InP, 80–140°C with GaAs and GaP, and below 30°C with AlSb and GaSb, as seen in Figure 2-1(a)–(d). GaN has also been etched with the technique, as shown in Figure 2-1(e).

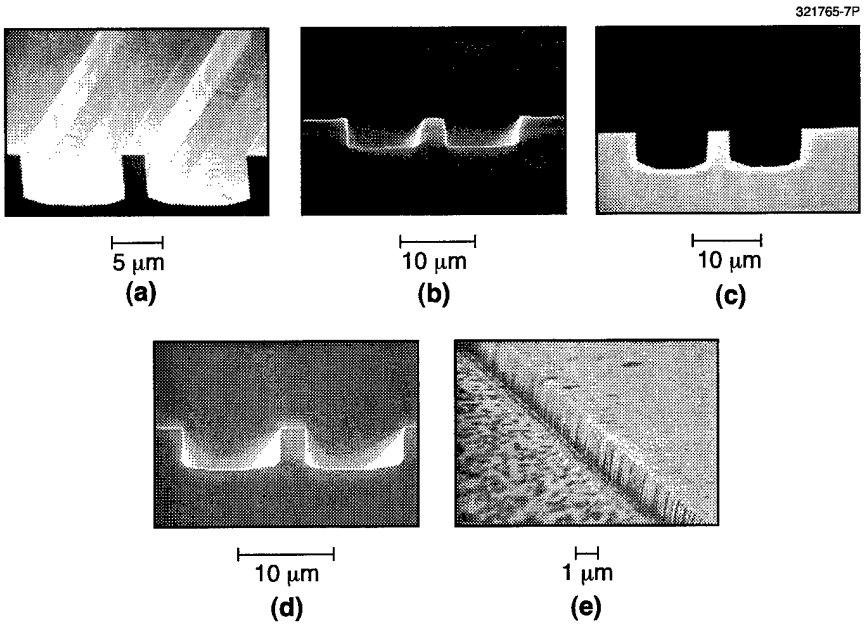


Figure 2-1. Micrographs of various III-V binaries etched with Br_2-IBAE: (a) GaAs at 100°C, (b) GaP at 100°C (photoresist mask still in place), (c) InP at 200°C, (d) GaSb at 20°C, and (e) GaN at 200°C.

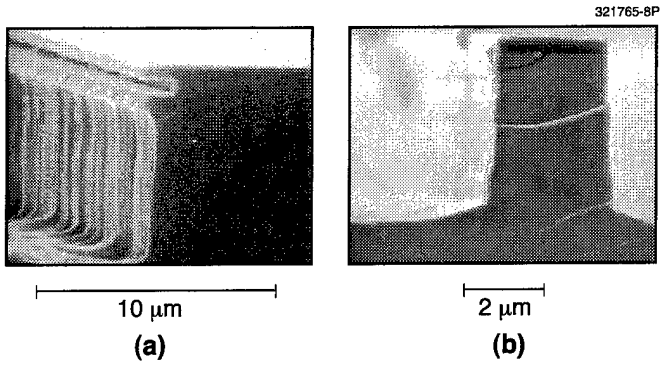


Figure 2-2. Micrographs comparing results obtained from etching GaAs/InGaP heterostructure with (a) Cl_2-IBAE at 175°C and (b) Br_2-IBAE at 115°C.

Our etching experience and the vapor pressure data for bromine with group III and group V elements lead us to believe that all of the various technologically important III-V binaries, ternaries, and quaternaries can be etched. Etch rates of most of the materials can be varied from several nm/min to 0.16 μm/min by changing the bromine flow rate, the Ar^+ ion beam density and energy, and the substrate temperature.

Br_2-IBAE also appears to have an advantage over Cl_2-IBAE in many situations in that substrate temperature ranges can be found for which vertical sidewalls are maintained while etching through layered structures composed of various alloys of the materials. For example, while Cl_2-IBAE spontaneously etches a GaAs layer clad with InGaP at a temperature of 175°C, the optimal temperature for etching vertical walls in InGaP with Cl_2, Br_2-IBAE nearly alleviates this problem when etching the same heterostructure at 115°C, the optimal temperature for etching vertical walls in InGaP with Br_2, as shown in Figure 2-2.

W. D. Goodhue
D. E. Mull
C. G. Fonstad*
Y. Royter
S. S. Choi

---

* Author not at Lincoln Laboratory.

2.2 PbTe/Te SUPERLATTICE STRUCTURES WITH ENHANCED THERMOELECTRIC FIGURES OF MERIT

General superlattice structures particularly suitable for use as thermoelectric materials have been described in [1]. An investigation of $Pb_{1-x}Eu_xTe$/PbTe quantum-well superlattices grown by molecular beam epitaxy (MBE) yielded an enhanced thermoelectric figure of merit in the quantum-well part ($Z_{2D}T$) of the material [2]–[4]. One problem with such structures is that the overall thermoelectric figure of merit ZT, which corresponds to both the barrier and well portions of the superlattice (SL), may be limited so that the ZT of these Pb-Eu-chalcogenide layered materials are, at best, only slightly improved over that of bulk thermoelectric materials. It is believed that the high $Z_{2D}T$ of the Pb-Eu-chalcogenide quantum wells is caused by quantum confinement [2]–[4], and the low ZT is caused by the relatively high thermal conductance of the PbEuTe barriers [2] and other effects [5]. At the beginning of this work, we assumed that the anomalously low thermal conductivity value of 2.4 mW/cm K at 300 K for EuSe in the *Handbook of Chemistry and Physics* [6] was correct. Subsequent unpublished measurements [7] using a high-quality bulk, high-electrical-resistivity single crystal of EuTe [8] yielded a value for the lattice thermal conductivity for EuTe of 110 mW/cm K at 300 K. Since both EuSe and EuTe have the rock-salt crystal structure, the *Handbook* value for the thermal conductivity of PbSe is incorrect [6]. Recently, we reported new and novel Pb-chalcogenide-based MBE-grown SL structures [9] with enhanced measured ZT, i.e., PbTe/Te and similar SL structures involving PbSeTe/PbTe/Te. The primary purpose of this report is to present the experimental results for the PbTe/Te SL structures.

It is well known that both PbTe and Te are semiconductors with comparable energy gaps and carrier mobilities. PbTe is isotropic, but Te is highly anisotropic. PbTe and PbSe have the rock-salt or NaCl crystal lattice, whereas Te has the trigonal lattice structure. Pure Te layers are intrinsic semiconductors at room temperature [10]. The electrical conductivity is anisotropic, being twice as great along the c-axis as perpendicular to it. At 300 K, the conductivity along the c-axis is approximately 3 $\Omega^{-1}cm^{-1}$. We have found that a thin adsorbed layer of Te can be inserted periodically in the PbTe lattice without altering the crystal structure, i.e., the NaCl crystal structure is retained as shown by in-situ reflection high-energy electron refraction (RHEED) and ex-situ x-ray diffraction measurements. Please note that typical adsorbed layers can be as thin as a partial monolayer or as thick as several monolayers. Small excesses of Te (greater than the solid solubility of excess Te in PbTe) are electrically neutral in the PbTe matrix and are present in the form of precipitates in bulk PbTe [11].

The PbTe/Te SL structures were grown by MBE, which provides monolayer control and excellent reproducibility. The MBE growth is being carried out in a modified Varian 360-type growth chamber with an associated custom-built load-lock chamber. The substrate is mounted on a molybdenum substrate holder with the use of an InGa alloy solder which is approximately at the eutectic composition of the alloy. The effusion cells on the cell flange used for the growth of PbTe/Te SL structures contain PbTe, $Bi_{0.9}Sb_{0.1}$, and Te. The substrate manipulator contains the substrate holder, an internal fixed heater, and an ionization gauge to measure beam fluxes. The manipulator is on a horizontal axis and provides rotation along the axis of the manipulator. This rotation is used to shift the substrate from the "growth" to the "transfer" position.

The manipulator includes X,Y, and Z motions and allows the axis location to be adjusted with precision micrometers. The MBE substrate holder accommodates substrates with 18 × 18-mm-square shape.

The deposition chamber is equipped with monitoring RHEED in addition to beam flux and background-pressure nude Bayard-Alpert vacuum gauges. A 30-keV RHEED system (used at 12 keV) is currently employed during film growth to optimize and monitor the deposition. The electron beam is directed to the sample surface with small incidence angles of about 0.3°. RHEED streaks are observed throughout the growth runs. Molecular- and atomic-beam fluxes arriving at the substrate location can be monitored via the beam-flux ion gauge. The main flux measurement tool is the nude Bayard-Alpert gauge, mounted on the manipulator, by which it may be rotated into the substrate position. In this position the beams from the individual sources can be monitored and calibrated. Precise run-to-run control of composition requires precise knowledge of the PbTe and Te beam fluxes. The beam flux of the *n*-type dopant source $Bi_{0.9}Sb_{0.1}$ (in subsequent work Bi was used and found to behave in the same way) is adjusted and monitored by measuring the Hall coefficient. The growth rate is in the range 0.7–1.4 μm/h. The Hall carrier concentrations of the PbTe and PbTe/Te growth runs are calculated from the Hall coefficient. For the growth of the PbTe/Te SL structures, the Te shutter is open during the entire growth run whereas the PbTe and $Bi_{0.9}Sb_{0.1}$ dopant shutters are alternately opened and closed. A schematic cross section of the PbTe/Te SL structure along with the Bi-doped PbTe buffer layer and the BaF_2 substrate is shown in Figure 2-3. The films can be

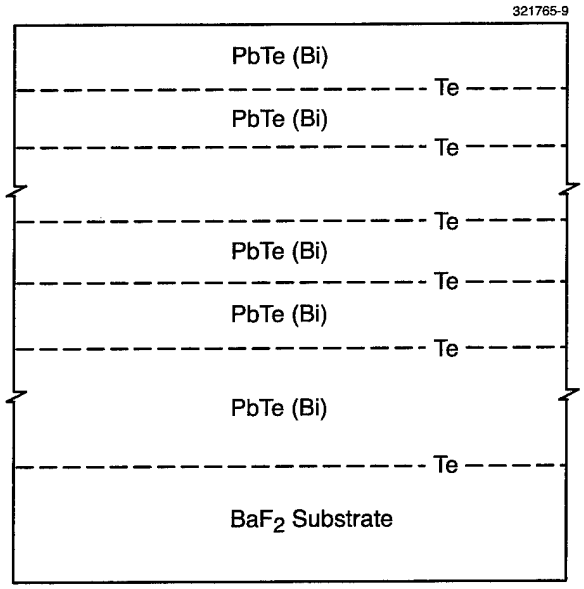


Figure 2-3. Schematic cross section of the PbTe/Te superlattice structure investigated.

removed from the electrically insulating BaF_2 substrate and used as thermoelectric chips for measurements or devices. The thicknesses of the Bi-doped PbTe sublayer were varied from run to run by changing the computer-programmed shutter times and/or by changing the effusion cell flux pressures between growth runs. At the growth temperature (325°C) and beam equivalent pressure (BEP) of the Te flux (approximately 2×10^{-7} Torr), the Te sublayer is an adsorbed layer and does not vary with effusion-cell shutter times or effusion-cell flux pressures in a simple manner. The PbTe-to-Te BEP flux ratio is in the range 8–12. At the end of the growth the surface of the film is shiny. The grown SL was cooled from the growth temperature to 250°C at 5°C/min and then annealed for 15 h at 250°C. The film/substrate structure was cooled from 250°C by turning the power off to the substrate. The in-situ RHEED patterns are streaked throughout the growth, indicating atom-layer-by-atom-layer growth.

The results for two high-quality (where high quality is defined as high mobility at both 77 and 300 K) epilayers of PbTe are given in Table 2-1. The measured period of the (Bi-doped PbTe/undoped Te) SL, the number of periods, and the Bi-doped PbTe buffer layer thicknesses of the films are given in Table 2-2. The thickness of the undoped Te layer has not been determined but is believed to be in the range 0.8–1.5 nm. The results of the properties of the PbTe/Te SL structures are given in Table 2-3. Notice that both the power factor and figure of merit of the best samples are significantly greater than the maximum value obtained for bulk or homogeneous film PbTe samples, as presented in Table 2-1.

The Seebeck coefficients of all samples listed in Table 2-2 are significantly greater than the values calculated from the empirical Seebeck coefficient S vs carrier concentration n relationship [2] obtained for bulk and homogeneous film PbTe at 300 K, i.e.,

$$S\ (\mu V/K) = -477 + 175 \log_{10}(n/10^{17}\ cm^{-3}) \quad . \tag{2.1}$$

It is believed that the primary cause of the Seebeck coefficient enhancement is the PbTe/Te structure shown in Figure 2-3. The Seebeck coefficient values of the PbTe/Te films are displayed in Figure 2-4 and

TABLE 2-1
300-K Thermoelectric Properties of Bi-Doped PbTe Films

Sample No.	Seebeck Coefficient (μV/K)	Power Factor (μW/cm K^2)	ZT*	Carrier Concentration n (cm^{-3})	Carrier Mobility μ (cm^2/V s)
T-184	–149	32	0.37	7.3×10^{18}	1200
T-253	–152	30	0.35	7.5×10^{18}	1060

*A literature value of the lattice thermal conductivity of 20 mW/cm K for PbTe at 300 K was assumed for all samples.

TABLE 2-2
Experimental Parameters of Bi-Doped PbTe/Te Superlattice Films

Sample No.	PbTe Buffer Thickness (nm)	Superlattice Period (nm)	No. of Periods
T-356	110	22	203
T-442	110	22	189
T-443	70	28	186
T-444	40	28	189
T-446	None	30	190
T-447	None	15	314

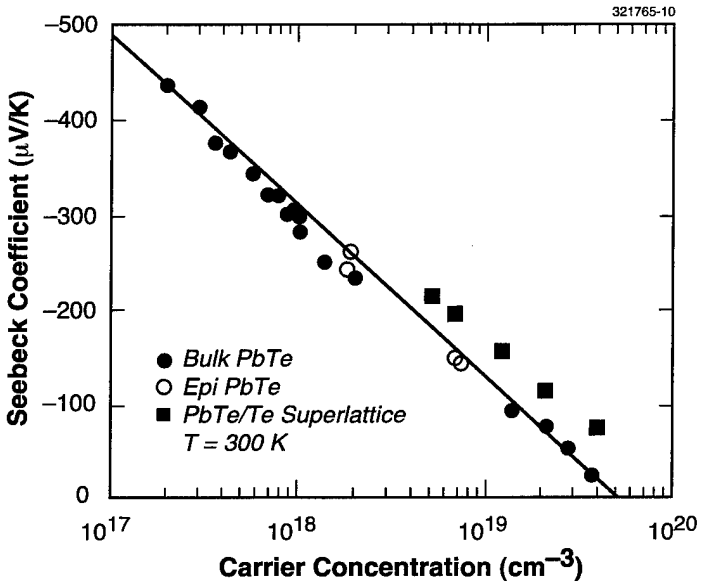


Figure 2-4. Seebeck coefficient vs carrier concentration for n-type bulk PbTe, epitaxial PbTe, and PbTe/Te superlattice structures.

show a decrease with increasing carrier concentration similar to that of bulk PbTe. The power factor $S^2\sigma$, where σ is the electrical conductivity, is listed in Table 2-3. These power factor values are presented in Figure 2-5 as a function of the carrier concentration at 300 K. The solid curve was calculated for bulk PbTe by fitting the bulk Seebeck coefficient and mobility data, and provides information near the optimum bulk carrier concentration of about 6×10^{18} cm^{-3}, where $S^2\sigma = 37–38$ $\mu W/cm\ K^2$ is expected. The power factor for the PbTe/Te SL films is significantly higher, for the same carrier concentration, despite their generally lower mobilities than bulk or homogeneous film PbTe. Notice that the maximum for the PbTe/Te power factor has shifted to higher carrier concentrations relative to bulk PbTe.

The thermoelectric figure of merit ZT or $S^2\sigma T/\kappa$, where κ is the thermal conductivity, is listed in Table 2-3. The ZT values are presented in Figure 2-4 as a function of the carrier concentration at 300 K. The solid curve for bulk PbTe was obtained from the power factor using thermal conductivity values calculated from lattice thermal conductivity values in the literature along with the Wiedemann-Franz law. The solid curve in Figure 2-6 provides information near the optimum bulk carrier concentration of about 6×10^{18} cm^{-3} where $ZT = 0.45$ is expected. ZT values for the PbTe/Te films are significantly higher (for the same carrier concentration) than either bulk or homogeneous film PbTe, and the optimum bulk carrier concentration for the PbTe/Te structures has shifted to higher carrier concentrations.

TABLE 2-3
300-K Thermoelectric Properties of Bi-Doped PbTe/Te Superlattice Films

Sample No.	Seebeck Coefficient ($\mu V/K$)	Power Factor ($\mu W/cm\ K^2$)	ZT*	Carrier Concentration n (cm^{-3})	Carrier Mobility μ ($cm^2/V\ s$)
T-356A	–177	44	0.50	8.3×10^{18}	1060
T-442A	–80	27	0.21	4.0×10^{19}	650
T-443A	–118	38	0.36	2.2×10^{19}	790
T-444B	–163	44.5	0.49	1.3×10^{19}	785
T-446A	–193	43	0.52	8.2×10^{18}	880
T-447A	–203	38.5	0.48	5.8×10^{18}	1015

*A literature value of the lattice thermal conductivity of 20 mW/cm K for PbTe at 300 K was assumed for all samples.

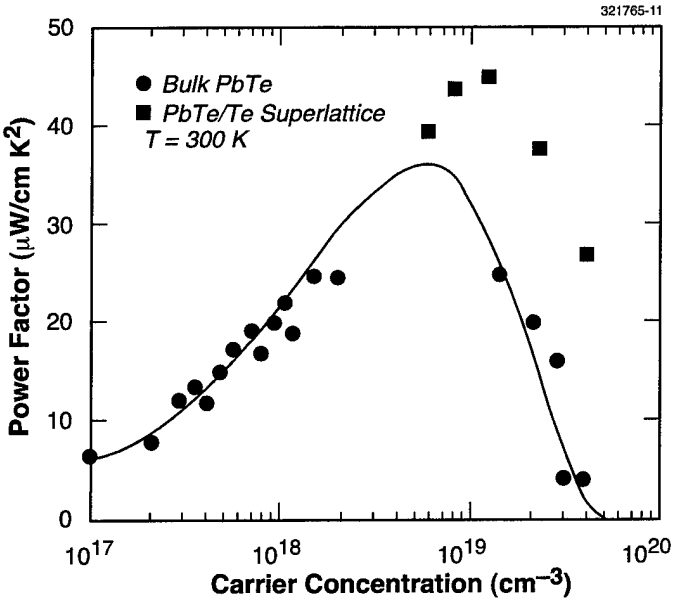


Figure 2-5. Thermoelectric power factor vs carrier concentration for n-type bulk PbTe and epitaxial n-type PbTe/Te superlattice structures.

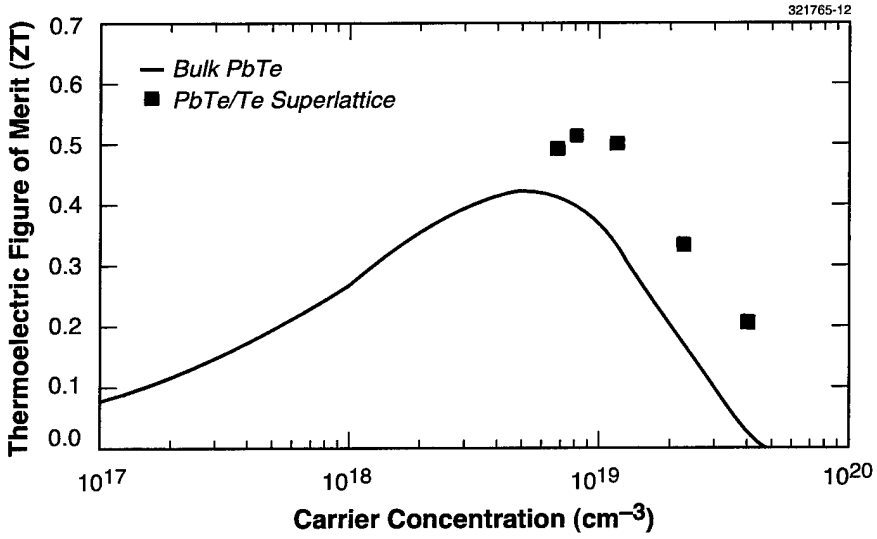


Figure 2-6. Thermoelectric figure of merit vs carrier concentration for n-type bulk PbTe and epitaxial n-type PbTe/Te superlattice structures, from measured power factor and calculated thermal conductivity.

In at least special cases, the momentum relaxation time $\tau_m(\varepsilon)$ [12],[13] takes the following form:

$$<\tau_m> \tau_o e^{r-1/2} \quad , \tag{2.2}$$

where e is the electron energy and r is the scattering parameter. The scattering parameter r is 0 for acoustical mode scattering, 1 for optical mode scattering, and 2 for impurity scattering. The Seebeck coefficient S can be written as

$$S = -k/e \{[(r + 2) F_{r+2}(\eta)/(r + 1) F_{r+1}(\eta)] - \eta \quad , \tag{2.3}$$

where k is the Boltzmann constant, e is the electronic charge, $F(\eta)$ is the Fermi-Dirac integral, and η is the ratio of the Fermi-level energy to kT. To a first approximation the Fermi-level energy determines the Seebeck coefficient as indicated in Equation (2.3). However, the second most important factor is the carrier scattering mechanism as manifested through the scattering parameter r in Equation (2.3). Therefore, one contribution to the measured enhanced in-plane Seebeck coefficient in the PbTe/Te SL structures is believed to be a more favorable scattering mechanism, which increases the value of the scattering parameter r. An increase in r results in an increase in S, as can be seen from the graphical display of S vs η for r = 0, 1, and 2 on page 199 of [12]. Please note that an r = 1/2 value in Equation (2.2) makes Equation (2.3) consistent with Equation (2.1). We speculate that the mechanism for explaining the enhanced ZT and S data for the PbTe/Te SL structures involves a resonance carrier-scattering (RCS) mechanism. This would explain why both shorter and longer period thicknesses do not appear to work as well. Since the distance between the Te adsorbed layers is much shorter than the mean free path of the conducting electrons, this indicates that quantum effects are involved. For the RCS mechanism the spacing and thickness of the Te layers may be important in optimally scattering charge carriers.

T. C. Harman
D. L. Spears
M. P. Walsh

2.3 MBE GROWTH OF HIGH-PERFORMANCE InAsSb/AlAsSb DOUBLE HETEROSTRUCTURES FOR MID-INFRARED OPSLS NEAR 4 μm

Semiconductor lasers that can emit in the mid-infrared wavelength region between 2 and 5 μm are useful for a variety of military and civilian applications. Lincoln Laboratory has been involved in a multi-year development effort to demonstrate high-power, quasi-cw semiconductor mid-infrared lasers for use in military infrared countermeasures systems. Compact, efficient, high-brightness semiconductor lasers, which can be integrated into existing directed energy countermeasure systems on military platforms, could be well suited to the task of jamming advanced infrared missile seekers. The technical approach has been to use our state-of-the-art, antimonide-based III-V MBE materials growth technology to grow high-performance mid-infrared quantum-well diode laser structures [14] wherever possible. In wavelength regions where high-power current-pumped diode lasers are not yet feasible, the alternative approach has been to grow semiconductor laser structures which are optically pumped [15]. In the optically pumped semicon-

ductor laser (OPSL) device configuration, shown in Figure 2-7, a conventional shorter-wavelength diode-laser pump array is used to optically pump a longer-wavelength semiconductor laser chip that is specifically designed for optical pumping. The OPSL approach has the advantages of elimination of the need for electrical current flow in the device, control of optical mode properties, and simplified fabrication. The major disadvantage of the OPSL approach is increased system complexity due to the requirement of a diode-laser pump array and associated pump focusing optics. Such mid-infrared OPSL chips, designed to emit near 4 μm, are cooled with a Sterling-cycle cooler to operating temperatures <100 K to minimize loss mechanisms and to maximize output power.

The results described here were obtained for OPSLs employing double-heterostructure (DH) designs of lattice-matched InAsSb active regions and AlAsSb cladding regions. These structures were grown in an EPI GEN II solid-source MBE system on *n*-type GaSb substrates. Two uncracked Sb_4 effusion cells were used in combination with an EPI valved As_2 cracking source in order to optimize the V/III ratios used for the growth of each alloy. Growth temperatures of 470–520°C were used, with no intentional doping of the *n*-type InAsSb active region and light *n*-type doping in the AlAsSb cladding layers, in order to achieve an *n-n-n* heterostructure for minimum free-carrier losses. The typical thicknesses of the lower cladding/active/upper cladding were 2/1.5/2 μm, respectively. A number of OPSL growths were performed on In-bonded GaSb substrates as well as whole nonbonded epi-ready 2-in. GaSb substrates. Excellent controllability and reproducibility of both emission wavelength and device performance were achieved. Post-growth processing consisted of backside thinning, antireflection coating for the pump wavelength, cleaving, mounting, and facet coating for 4-μm emission. For high-power operation, OPSL chips were mounted epi-side down on diamond heatsinks. Optical pumping was performed using both 0.98- and 1.9-μm pump arrays.

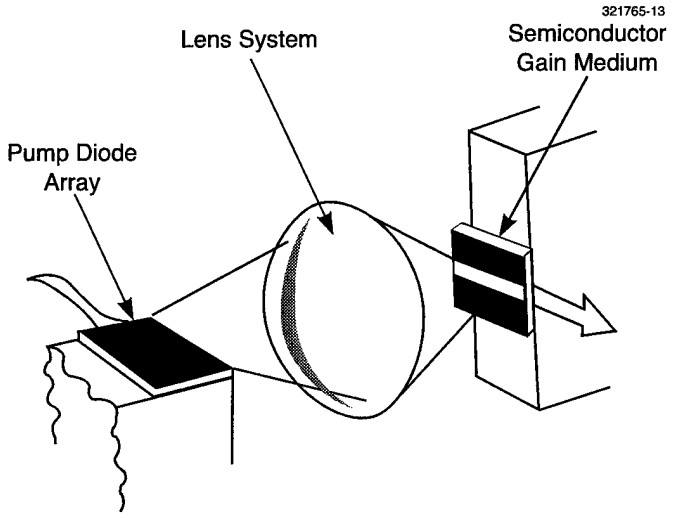


Figure 2-7. Schematic of optically pumped semiconductor laser (OPSL) pumping configuration.

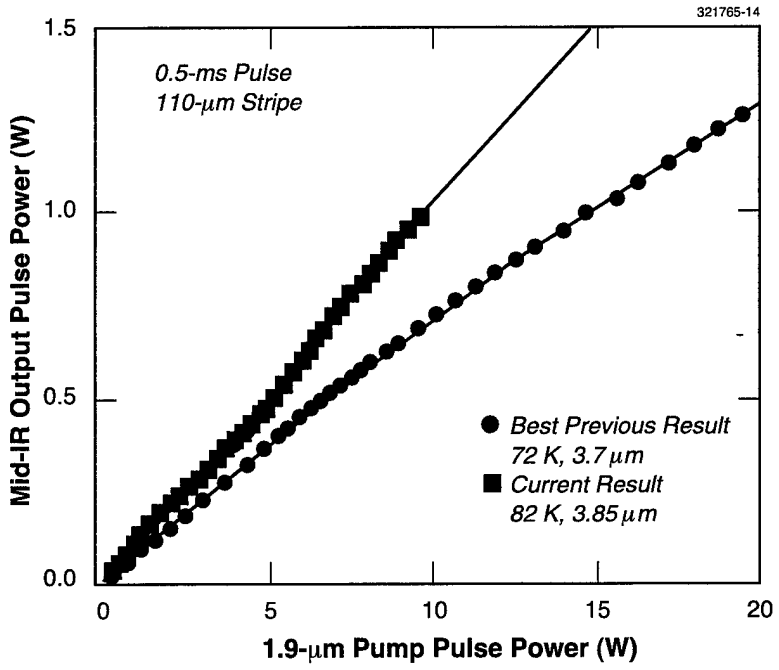


Figure 2-8. Mid-infrared pulse output power vs 1.9-μm input pump power for improved double heterostructure at 82 K and best previous result at 72 K.

Figure 2-8 shows our best OPSL result obtained with 1.9-μm pumping. At 82 K we obtained 0.95-W pulse output (0.5 ms at 100 Hz) at 3.85 μm, with 10-W pump input, yielding an optical-to-optical power conversion efficiency of 9.5%. This value significantly exceeds the ~6.5% conversion efficiency we had previously obtained at 72 K and is a new performance record for a mid-infrared OPSL. Output-beam quality measurements were also performed on this device and a value of 51 mm-mrad achieved. Such excellent performance can only be obtained with high-quality DH material, and we estimate that this OPSL device exhibited optical loss of ~8 cm^{-1} and internal quantum efficiency of >55%. The characteristic temperature T_0 of these devices is estimated to be ~20 K, although the ultimate high-temperature performance of these DH OPSLs may be more limited than what is projected for advanced quantum-well OPSL structures.

The excellent output power, power conversion efficiency, and brightness results that we have obtained with 4-μm DH OPSLs operating at 80 K satisfy the near-term technical requirements of an effective Sterling-cycle-cooled mid-infrared countermeasure system. With further advances in the MBE growth of mid-infrared quantum-well structures, we hope to further increase the maximum operating temperatures of high-performance OPSLs.

G. W. Turner
M. J. Manfra
J. L. Daneau
H. Q. Le
C. Cook
S. Buchter

2.4 ALIGNMENT OF MASS-TRANSPORTED MICROLENSES WITH TAPERED DIODE LASERS AND TAPERED-LASER ARRAYS

Improved techniques for alignment and attachment of mass-transported microlenses [16],[17] directly onto the facets of diode lasers are described. These techniques provide accurate positioning which is sufficient to maintain near-diffraction-limited optics when used with astigmatic tapered lasers [18] and tapered-laser arrays. The output beam of a lens can be collimated or focused to a spot which, at least for single lasers, permits efficient coupling of the beam into a single-mode optical fiber. Anamorphic mass-transported microlenses have been previously designed, fabricated, and shown to correct the astigmatism of tapered lasers with up to 30% of the total laser power coupled into nearly ideal beams [19],[20]. In these earlier experiments the lenses were actively aligned using high-quality optical positioners during the evaluation, rather than permanently affixed to the lasers. The use of mass-transported lenses mounted directly onto the surface of diode laser facets has been previously described [21] for single-element diode lasers having ridge-waveguide stripe-geometry cavities, and hence little or no astigmatism in the output beam.

In order to maintain near diffraction-limited optics, the positioning of a single element or laser array during soldering to the heatsink and the subsequent alignment of the microlenses are extremely critical and must be controlled accurately. Figure 2-9 shows the six degrees of freedom, the linear and angular displacements x, y, and z and ϕ, θ, and ψ, which must be controlled throughout the packaging, both for the microlenses relative to the lasers and the lasers relative to the laser heatsink. Two other alignment issues are also illustrated: a small overhang of the laser diode output facet with respect to the edge of the heatsink, and flatness of the wafer in the plane of the laser junction.

The overhang, the rotation about the y axis (θ or yaw), and the flatness must be controlled during the soldering of the diode to the heatsink. Since the devices are generally mounted junction-side down, an overhang is necessary in order to ensure that the edge of the heatsink does not interfere with the optical output beam from the laser. However, the overhang must be kept at a minimum for two reasons. If the overhang is too large the heatsinking process will be jeopardized. Also, during the second phase of the packaging when the microlenses are aligned and attached, there is a fixed rotation of the microlens about the x axis (the fixed pitch ϕ_f, shown in Figure 2-9), which is determined by the overhang h and the length of the microlens. The fixed pitch is designed to be $<0.5°$, which causes a small but tolerable degree of beam steering. The lens-alignment scheme requires that the microlens rest against the laser and its heatsink, making contact with the facet of the laser along the entire length of the emitting region. Therefore, for large output facets and especially for arrays, minimal yaw is important. This yaw is most easily measured by the uniformity of the overhang, i.e., from the difference observed in the overhang at the two sides of the output facet. Flatness is also most important when laser arrays are involved. Nonuniform pressure on the wafer during soldering can lead to deformation of the wafer similar to that indicated in Figure 2-9(c), which is often referred to as smile because of the characteristic shape of the deformation. If smile occurs, accurate alignment of a linear array of microlenses will not be successful.

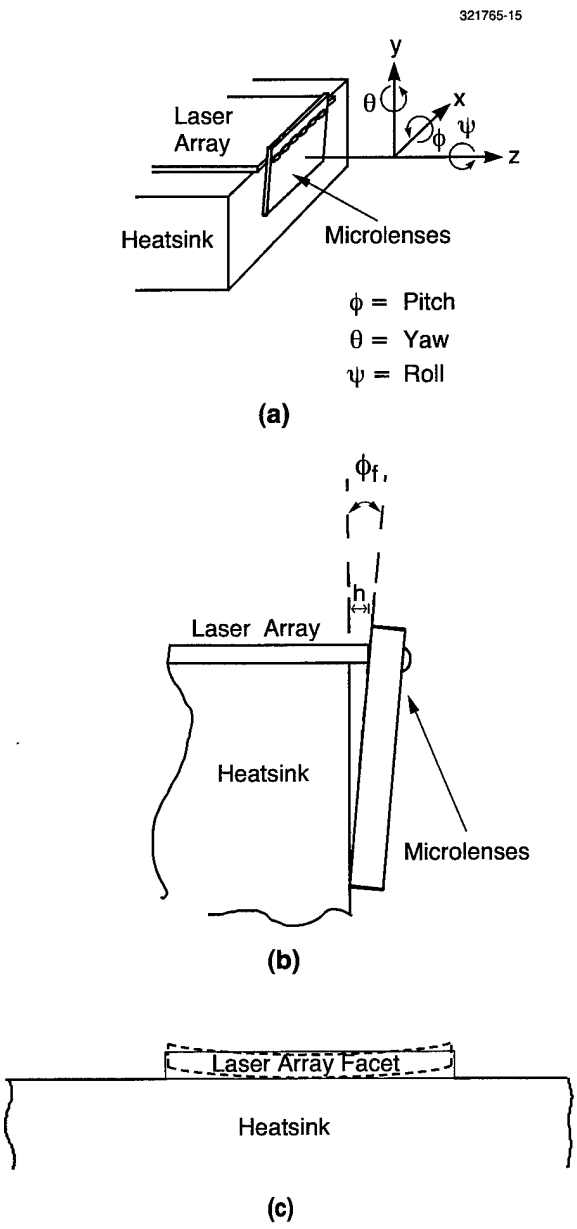


Figure 2-9. (a) Perspective view of microlens array positioned in front of laser array chip on heatsink. The linear and angular degrees of freedom, as used in the text, are defined here. (b) Side view of microlens array showing fixed pitch ϕ_f caused by overhang h. (c) Illustration of flat wafer (solid lines) as seen from the facet vs wafer lacking flatness (dotted lines). The deformation depicted is known as smile.

As shown in Figure 2-9, the z axis is the optical axis of the laser-lens system. The relative position of the microlens with respect to the laser in the z direction, and hence the focal point or points in the case of an anamorphic lens, is determined by the thickness of the lens, since the lens is in contact with the laser facet. Accurate control of the thickness can be achieved by polishing the microlens wafer to the desired thickness. Precise positioning of the lens in the x-y plane along with minimum rotation about the z axis (ψ or roll) is required during the lens alignment stage of the packaging. The techniques described below represent a simple and novel approach for achieving all the requirements for alignment accuracy discussed here.

Figure 2-10 shows the technique used to position the laser wafer accurately with respect to the heatsink to which it is to be soldered. Two pieces of GaAs are shown, the GaAs spacer and the GaAs cover. These pieces can be made from Si or some other convenient single-crystal material that can be accurately ground to achieve flat surfaces, accurately cleaved with high precision, and can be patterned and etched using photolithographic masking techniques. The latter is used to form the step in the spacer, which will determine the overhang of the laser relative to the edge of the heatsink. This step height or overhang was selected to be either 5 ± 1 or 10 ± 1 μm for the experiments described here. The GaAs cover also has an etched step that is approximately 30 μm deep.

The heatsink, laser wafer, spacer, and cover are assembled as shown in Figure 2-10. There is a packaging jig, not shown, that simply holds the spacer and the heatsink together throughout the alignment and soldering of the wafer. As stated above, the step in the spacer determines and controls the overhang of the laser facets with respect to the substrate. For reasons noted earlier, it is important that the output facets

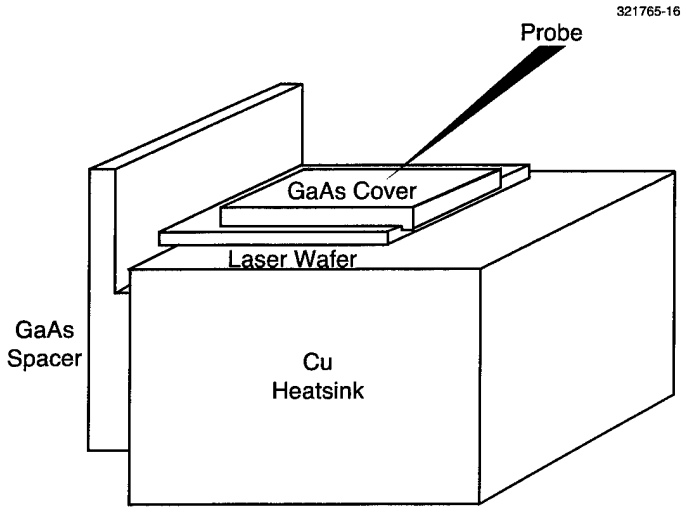


Figure 2-10. Perspective view of mounting scheme used to align and hold laser wafer during soldering to heatsink. Specifications: overhang, 2–7 μm; yaw, <1 μm; smile, <0.5 μm.

extend slightly beyond the edge of the heatsink. An overhang up to 10 μm appears to be acceptable in this regard. The probe shown in the figure is used to push the cover so that it, in turn, pushes the wafer into contact with the spacer, assuring accurate control of the overhang and parallelism of the facet and the edge of the heatsink (uniform overhang).

The cover piece also plays another important role when the wafer consists of an array of lasers. In the latter case, the cover distributes the pressure of the probe so that the wafer is not distorted during the soldering process, i.e., the wafer is not bowed into the solder at the center. Hence, the deviation from a straight line of the elements of the array can be avoided. This is the issue of the control of the smile previously discussed. The deviation from a straight line was kept less than about 0.5 μm for arrays of up to 9 elements extending over about 2-mm total facet length, using the GaAs cover during soldering with In solder at 160°C. Except for occasional instances in which there was noticeable motion (slipping) of the various elements depicted in Figure 2-10 during the soldering operation, the overhang was generally uniform within about 1 μm and slightly less than the step height for the spacer. Typically, about 2–4-μm overhang was observed for the nominally 5-μm spacer and about 7–9 μm for the nominally 10-μm spacers.

Figure 2-11 illustrates the technique for positioning the microlens array relative to the laser array after the latter has been soldered to the heatsink and wirebonds have been attached to achieve electrical contact. The heatsink is attached to a larger thermoelectrically cooled heatsink and positioned under an infrared/visible microscope. The laser facets are pointed directly upward towards the microscope. The laser array on its heatsink and the larger heatsink are all attached to a plate which can be positioned in the x and y directions, shown in Figure 2-11, with accuracy of 0.1 μm using a commercial feedback-controlled micropositioner. The plate can also be rotated in the x-y plane with an angular accuracy of $<0.5°$. The microlens array is held by a vacuum wand attached to another positioner that permits ordinary x, y, and z micrometer-controlled motion. As mentioned above, a microscope and camera which can see both visible and infrared images is used to monitor the microlens alignment. The microlens is initially aligned in the near field. The edge of the laser array which contains the active devices is positioned so that it is parallel and collinear to the center of the lenses on the lens array, i.e., the edge of the laser array bisects all of the lenses in the microlens array. Once the initial alignment has been completed, the lasers are biased above threshold. By adjusting the focus of the microscope, the near-field and far-field patterns of the laser output can be observed. Alignment adjustments are made using the micropositioning equipment to ensure symmetry of the near-field and far-field patterns. The microlens is incrementally lowered as the alignment is performed until it is resting on the facet of the laser array. Once the alignment has been completed, a probe is lowered onto the lens array to secure its position so that epoxy can be applied. The epoxy is delivered to the base of the lens array using a second probe. The epoxy is allowed to wick up the sides of the lens array and then cured with a uv light source. Once the lens array is secured, the vacuum wand is released and the initial probe is lifted.

The technique for the alignment of a tapered laser to a single-mode optical fiber makes use of a single anamorphic lens which was designed to focus the output of the tapered laser to a spot that is comparable to the waist of the fiber mode. Such lenses have been reported [20] and preliminary results using this technique have also been reported [22], but the technique itself has not been previously described.

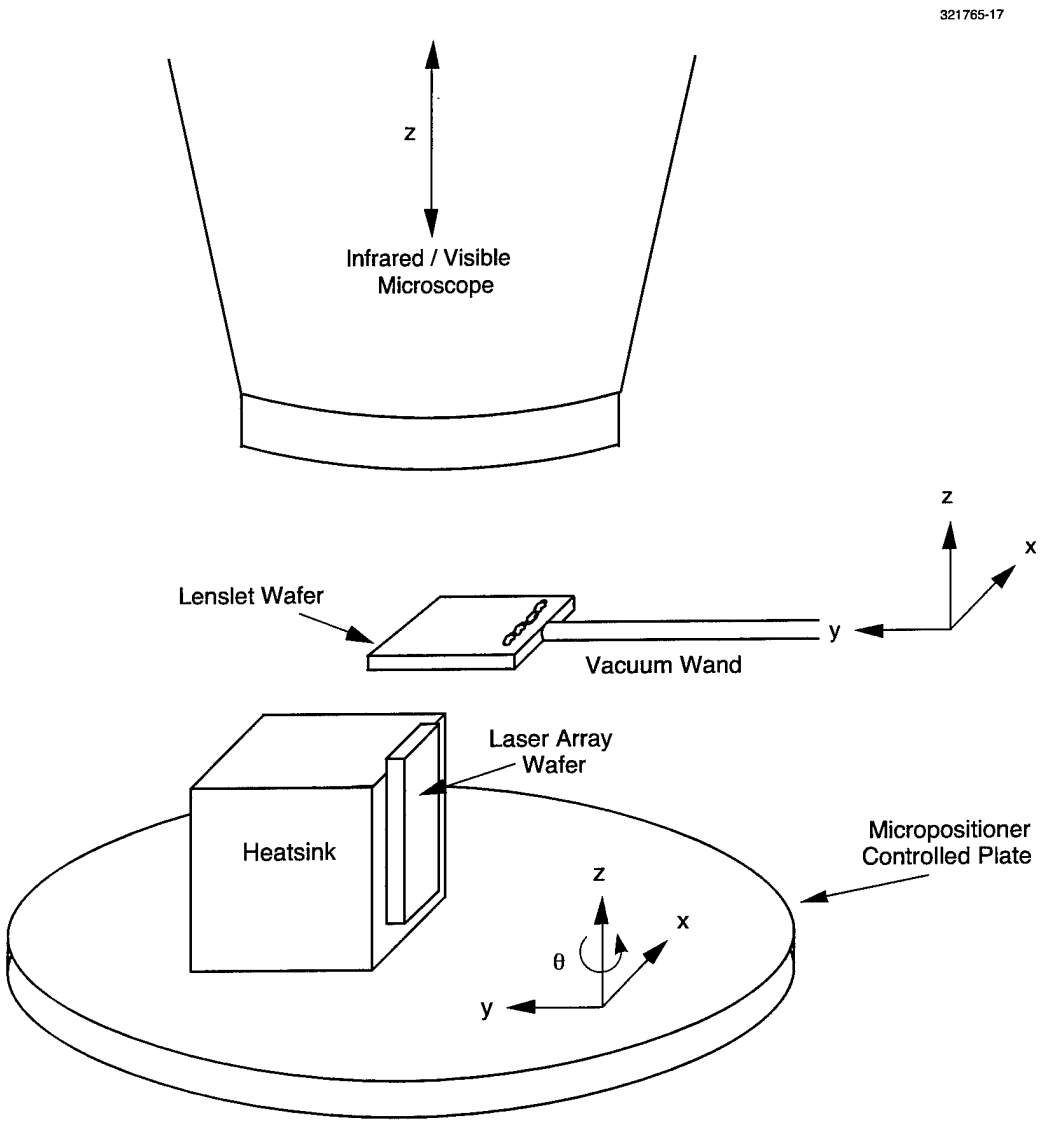


Figure 2-11. Perspective view of apparatus used to align and hold microlenses with respect to mounted laser prior to and during attachment with epoxy.

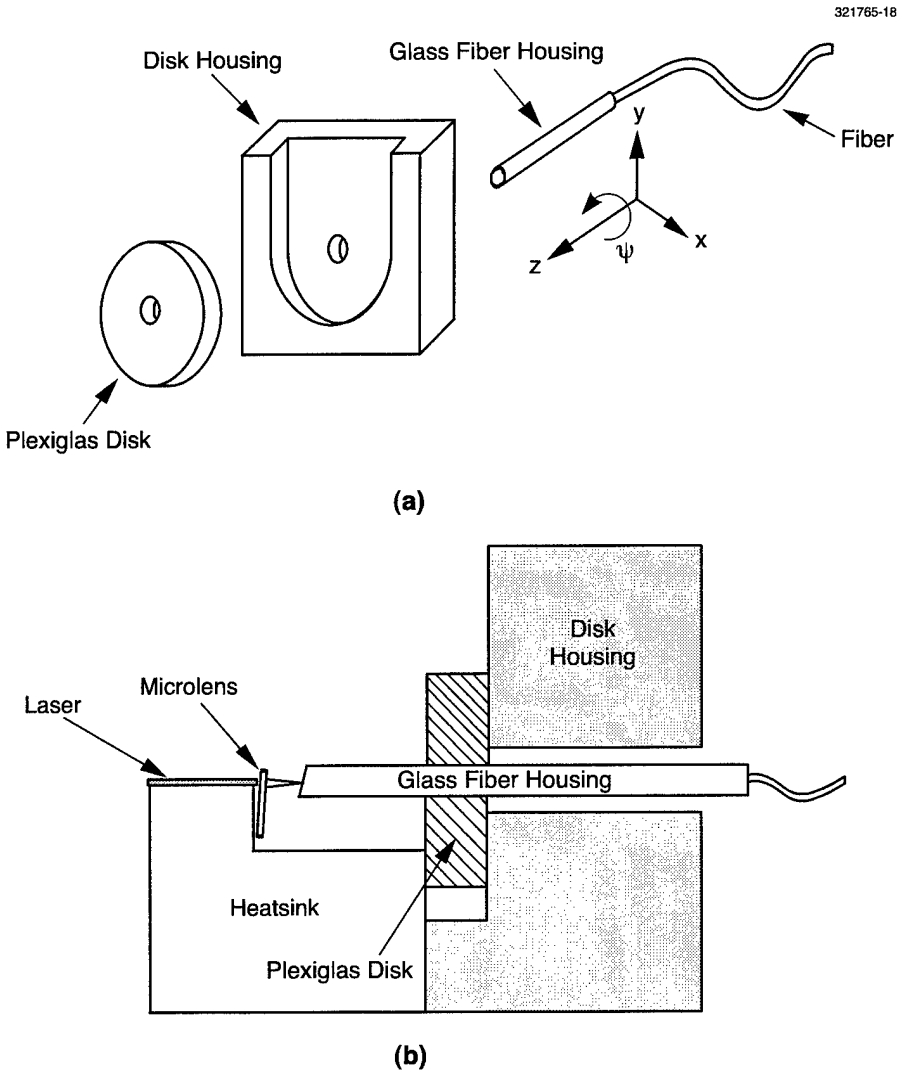


Figure 2-12. (a) Components of fiber-holding apparatus shown in perspective. (b) Cross-sectional view of same components assembled with laser, microlens, and heatsink.

Figure 2-12 shows a schematic of the holder for the single-mode fiber which is designed to allow separate alignment of the fiber in the x and y planes, the z direction, which as before is the optical axis of the laser, and the angular orientation about the z direction. The fiber was first put into a cylindrical glass fiber housing, obtained from AT&T, which has a capillary tube through its center for threading the fiber. The fiber was epoxied into the housing using the same uv curing epoxy discussed above. The fiber and the glass housing were then polished to obtain a flat end on the fiber which was at a small angle (about 12°) to

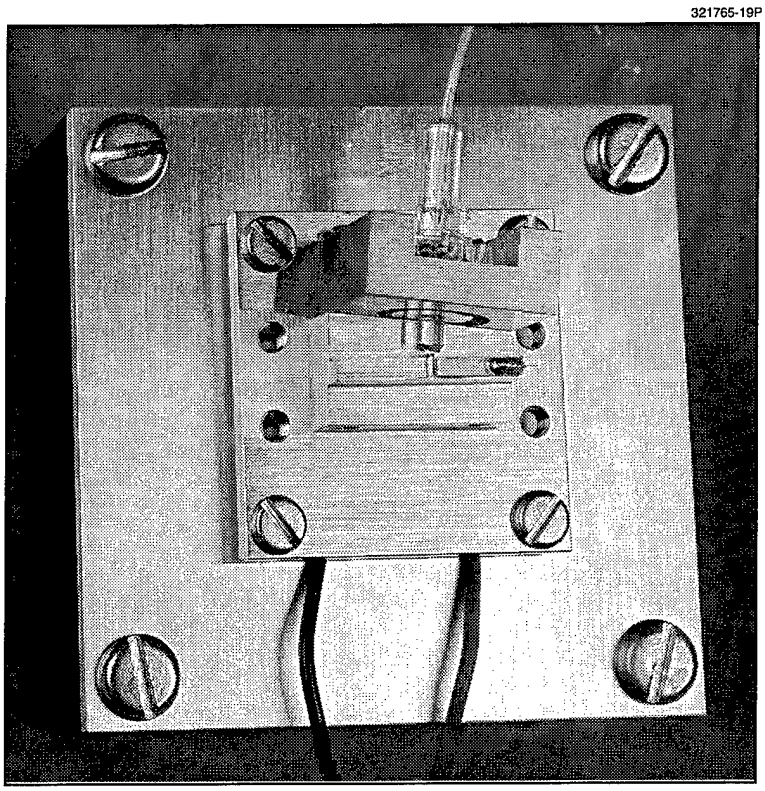


Figure 2-13. Photograph of assembled package with laser, microlens, and fiber all rigidly attached and aligned.

the fiber axis to eliminate optical feedback from the fiber to the laser. For this reason, angular orientation about the z direction is necessary. (Because of this angle, there is some interaction between positioning in the x-y plane and positioning along the z axis but, to first order, it is of little practical consequence.)

The Plexiglas disk, shown in Figure 2-12, is placed within the milled region of the disk housing, which is then attached to the laser heatsink to which the laser has been soldered. Plexiglas was used because it is easily machined and transmits the uv light. The disk housing is machined so that the Plexiglas disk can fit within the circularly milled area with good clearance (about 30 μm) between the disk and the heatsink. This allows lateral motion in the x-y plane of the disk with respect to the housing and heatsink. The glass fiber housing holding the fiber is aligned through the disk housing and the Plexiglas disk using an x, y, z micropositioner. Epoxy is applied to the shaft of the fiber housing and the back side of the disk. When the fiber alignment has been completed and the maximum optical power coupled into the fiber has been achieved, a uv light source is applied to cure the epoxy and freeze the assembly in place.

Figure 2-13 is a photograph of such an assembly seen looking down at the top of a laser mounted on a heatsink to which the disk housing has been attached. The fiber has been aligned and attached with

epoxy. Note the small angle between the actual fiber axis and the laser axis. Up to about 60% of the total power from a tapered laser mounted in this way was successfully coupled into the single-mode fiber at 980 nm [22].

L. J. Missaggia
J. N. Walpole
Z. L. Liau

REFERENCES

1. T. C. Harman, "Superlattice Structures Particularly Suitable for Use as Thermoelectric Cooling Materials," U.S. Patent No. 5,415,699 (16 May 1995).
2. T. C. Harman, D. L. Spears, and M. J. Manfra, *J. Electron. Mater.* **25**, 1121 (1996).
3. L. D. Hicks, T. C. Harman, X. Sun, and M. S. Dresselhaus, *Phys. Rev. B* **52**, R10493 (1996).
4. T. C. Harman, D. L. Spears, D. R. Calawa, S. H. Groves, and M. P. Walsh, *Proceedings of XVI International Conference on Thermoelectrics* (Dresden, Germany, 1997), p. 416.
5. See for example, T. L. Reinecke, and D. A. Broido, *Proceedings of XVI International Conference on Thermoelectrics* (Dresden, Germany, 1997), p. 424, and references therein.
6. L. I. Berger and B. R. Pamplin, eds., "Properties of Semiconductors," in *Handbook of Chemistry and Physics*, 74th ed., D. R. Lide, ed. (CRC, Boca Raton, Fla., 1993-1994).
7. R. O. Pohl and E. Wahang, private communication by G. A. Slack.
8. Grown at Lincoln Laboratory by R. E. Fahey.
9. T. C. Harman, M. P. Walsh, and D. L. Spears, to be published in *J. Electron. Mater.* **27**(7) (1998).
10. P. Grosse, *Solid State Properties of Te*, Vol. 48 of *Springer Tracts in Modern Physics*, G. Hohler, ed. (Springer, New York, 1969).
11. T. C. Harman, *J. Nonmetals* **1**, 183 (1973).
12. T. C. Harman and J. M. Honig, *Thermoelectric and Thermomagnetic Effects and Applications* (McGraw-Hill, New York, 1967), p. 193.
13. K. Seeger, *Semiconductor Physics: An Introduction* (Springer-Verlag, Berlin, 1997), p. 49.
14. G. W. Turner, H. K. Choi, and M. J. Manfra, *Appl. Phys. Lett.* **72**, 876 (1998).
15. H. Q. Le, G. W. Turner, and J. R. Ochoa, *IEEE Photon. Technol. Lett.* **10**, 663 (1998).
16. Z. L. Liau, D. E. Mull, C. L. Dennis, R. C. Williamson, and R. G. Waarts, *Appl. Phys. Lett.* **64**, 1484 (1994).
17. J. S. Swenson, Jr., R. A. Fields, and M. H. Abraham, *Appl. Phys. Lett.* **66**, 1304 (1995).

18. E. S. Kintzer, J. N. Walpole, S. R. Chinn, C. A. Wang, and L. J. Missaggia, *IEEE Photon. Technol. Lett.* **5**, 605 (1993).

19. Z. L. Liau, J. N. Walpole, D. E. Mull, C. L. Dennis, and L. J. Missaggia, *Appl. Phys. Lett.* **64**, 3368 (1994).

20. Z. L. Liau, J. N. Walpole, J. C. Livas, E. S. Kintzer, D. E. Mull, L. J. Missaggia, and W. F. Dinatale, *IEEE Photon. Technol. Lett.* **7**, 1315 (1995).

21. Z. L. Liau, D. Z. Tsang, and J. N. Walpole, *IEEE J. Quantum Electron.* **33**, 457 (1997).

22. F. Durville, R. H. Rediker, Z. L. Liau, J. N. Walpole, L. J. Missaggia, and W. F. Sharfin, presented at Tenth Annual Diode Laser Technology Review, USAF Phillips Laboratory, Albuquerque, N.M., 1997.

3. SUBMICROMETER TECHNOLOGY

3.1 AERIAL IMAGE EFFECTS ON LINE-EDGE ROUGHNESS IN TOP-SURFACE IMAGING RESIST

Top-surface imaging (TSI) technologies [1] are candidates for future high-resolution patterning, either to extend optical lithography (such as 193 nm) to the smallest dimensions possible, or as a main resist alternative for post-optical lithographies such as extreme uv or low-energy electron imaging. However, the high level of edge and surface roughness exhibited by both chemically amplified (CA) and non-CA TSI resists becomes problematic as critical dimensions (CD) shrink to 130 nm and below. Linewidth variations caused by 5–10 nm of line-edge roughness (LER) will consume an increasing amount of the CD tolerance budget, may decrease the process latitude, and can degrade device performance, uniformity, and ultimately wafer yield.

One important class of TSI resists are the silylated resists which are treated with a silicon-containing vapor prior to plasma development, as illustrated in the process flow shown in Figure 3-1. Silicon, which is incorporated into the unexposed resist regions, acts as an in-situ etch mask when patterning the underlying resist layer. In these resists poor mask edge definition related to stochastic processes during exposure, and varying silicon content after silylation, are the dominant factors contributing to the formation of line-edge and surface roughness. Figure 3-2 shows a plot of measured surface roughness in poly(4-hydroxystyrene) (PHOST) resist prior to plasma development as a function of exposure dose. At low exposure doses the silylation proceeds deep into the resist film, and at high exposure doses silylation is prevented by crosslinking of the resist. In both cases the resist remains relatively smooth. However, at the transition region between high and low doses the amount of silylation varies and large amounts of surface roughness are observed.

This variation of surface roughness with exposure dose is interpreted as evidence of an inhomogeneous response in the resist stemming from a statistically insufficient number of chemical events per pixel. The manifestation of such statistical underexposure could vary significantly as a result of resist chemistry (contrast, reaction order, acid diffusion, etc.), and too little data currently exists to develop a fully quantitative model. Nevertheless, if one could qualitatively look at an exposure aerial image, one would observe that the lateral dimension of resist exposed to this "statistically challenged" dose varies directly with the inverse of the image-log slope, as outlined schematically in Figure 3-3. The image-log slope is related to the nanoscale variations in the silicon content and the silylation depth at the feature edge. This in turn affects the feature size on a nanometer scale to result in LER.

The effects of exposure dose and aerial image on LER have been investigated experimentally by patterning nominal 175-nm isolated line features using a 193-nm optical stepper [2] with 0.5 numerical aperture and partial coherence of 0.6. The wafers were silylated to a nominal depth of 300 nm in a vapor silylation system using dimethylsilyldimethylamine (DMSDMA) as the silylating agent [3]. Wafers were dry developed in a high-density, low-pressure transformer-coupled plasma etch tool [4]–[5] using a

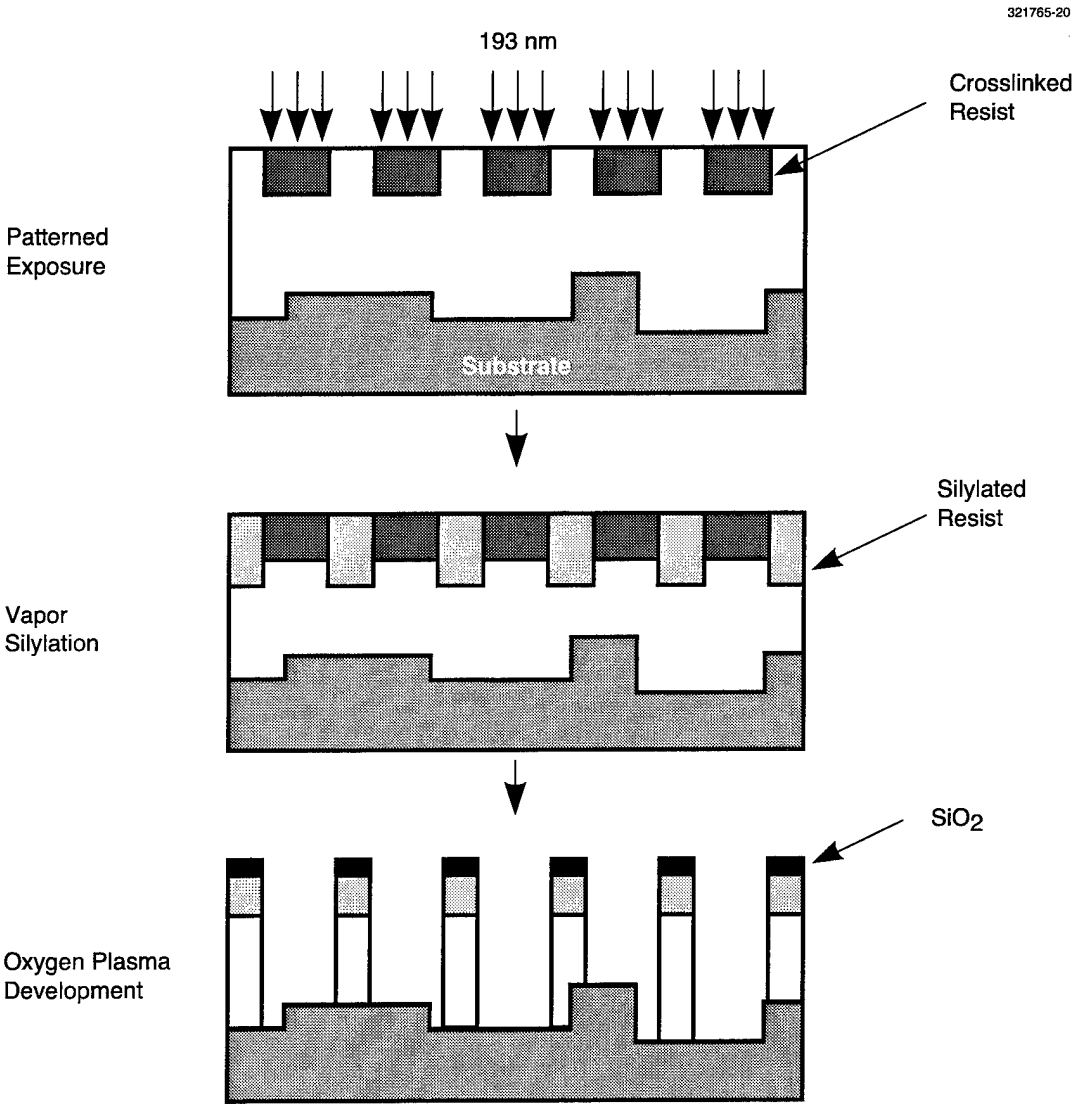


Figure 3-1. Process flow for silylated top-surface imaging resist, such as poly(4-hydroxystyrene) (PHOST).

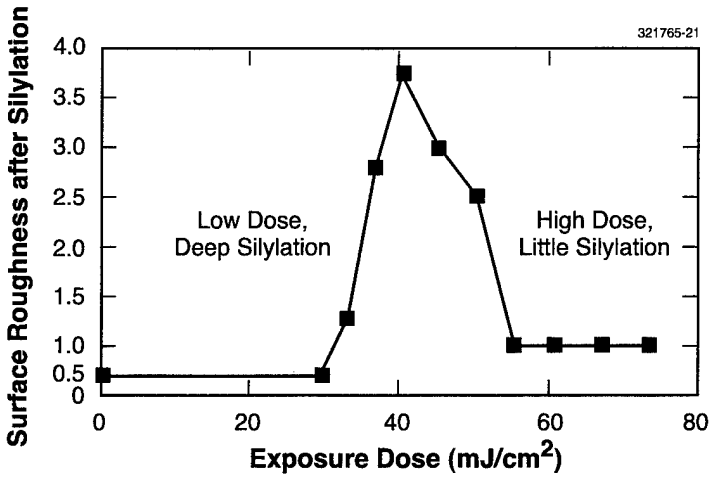


Figure 3-2. Surface roughness (total indicated range) of exposed and silylated PHOST plotted as a function of exposure dose. These samples were exposed and silylated but not developed in the oxygen plasma.

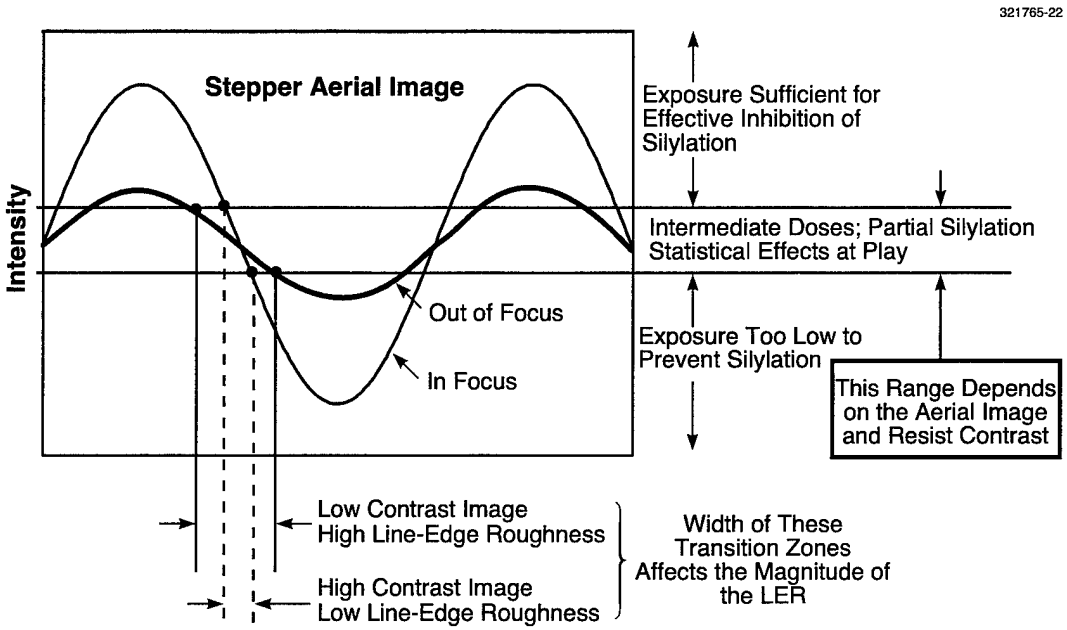


Figure 3-3. Schematic linking aerial image contrast to line-edge roughness (LER). Aerial image regions with high intensity correspond to high-dose regions in Figure 3-2, whereas those with low intensity correspond to low-dose regions. The transition region demonstrates the most surface and LER. The width of the transition region is proportional to the inverse of the image-log slope.

TABLE 3-1
Two-Step Dry Etch Process

Parameter	O_2 Dry Development	
Etch Step	**Breakthrough Etch**	**Main Etch**
Source power (W)	150	275
Chuck power (W)	25	250
Chemistry	C_2F_6/O_2	O_2
Flow (sccm)	15/15	60
Pressure (mTorr)	5	5
Selectivity		
Sily/unsily	0.8:1	30:1
SiO_2/resist	–	100:1
Temperature (°C)	–30	–30
Uniformity (blanket wafers)	–	6%

two-step dry etch process, as described in Table 3-1. Top-down scanning electron micrographs (SEMs) at several locations, shown in Figure 3-4(a),(b), illustrate the increase in LER with defocus and the decrease in LER with exposure dose. Figure 3-4(c) plots the experimental contours of LER along with the contour describing a +/–10% feature size variation. The intersection of these contours describes the process window and illustrates that the 10% CD control requirement constrains the allowable dose variation in this process, but a requirement of <3 nm of LER limits the allowable focus variation.

Modeling of the inverse image-log slope through dose and focus shows behavior identical to experimental results for the same exposure conditions. Figure 3-5 shows the calculated values of the inverse image-log slope in the dose-focus plane. This suggests that, at least for PHOST, whatever mechanism leads to LER is exacerbated at low image contrast. Even this qualitative observation would be useful in determining limiting performance for low k-factor lithography. For example, the measured LER exceeds 2 nm rms for image-log slope with values less than 10 or so for this PHOST process. This information can be very useful when projecting the performance and limits of future resist technologies.

S. C. Palmateer
R. R. Kunz
T. M. Lyszczarz
M. B. Stern
T. Fedynyshyn

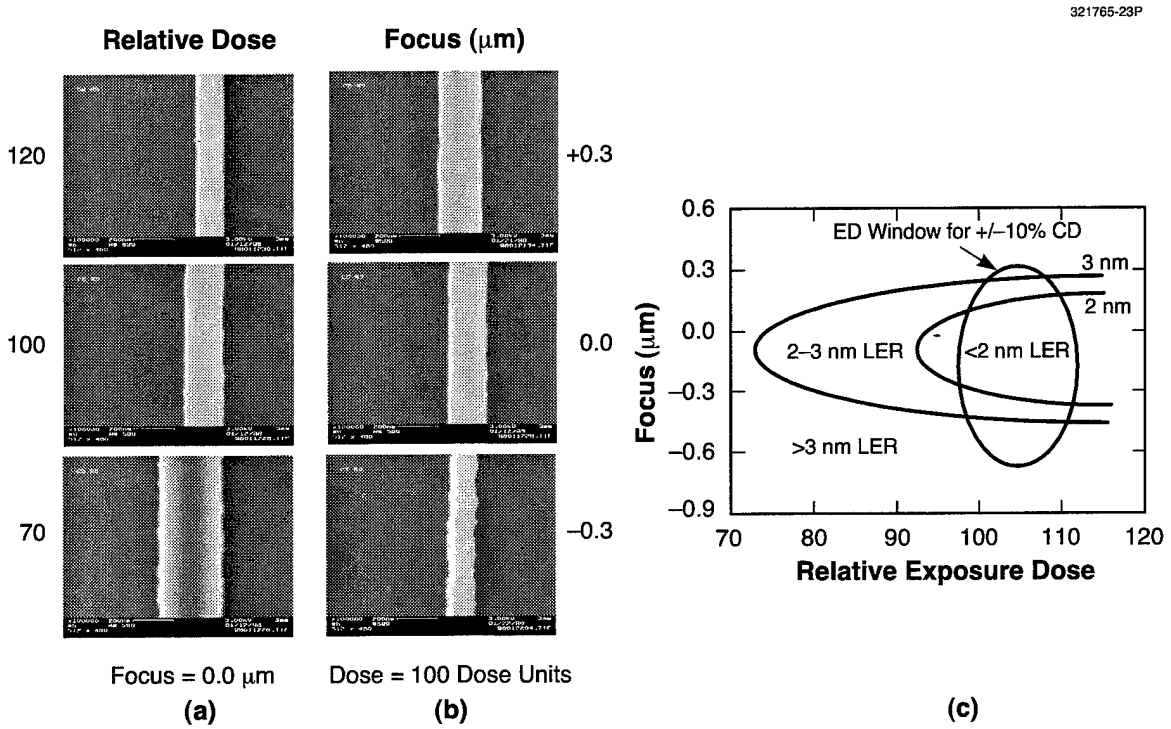


Figure 3-4. Process latitude: LER variation with exposure and focus. (a) Effects of dose variation at best focus. (b) Effects of focus variations at best dose. (c) Pictorial representation of process window.

3.2 PECVD THIN FILMS FOR MEMS APPLICATIONS WITH TAILORED OPTICAL, THERMAL, AND MECHANICAL PROPERTIES

Plasma enhanced chemical vapor deposition (PECVD) has been used very successfully in integrated circuit fabrication for dielectric films. For microelectromechanical systems (MEMS) applications it is an ideal deposition method because, unlike sputtering or evaporation deposition techniques, films can be deposited on surfaces that are not in the line of sight. Previously, we have shown how PECVD can be used for planarizing topographic substrates [6] and for synthesizing photoresists [7],[8]. Here, we demonstrate the ability to tailor many of the critical film properties for a particular MEMS application: microbolometer detectors for uncooled infrared focal plane arrays [9].

Currently, several companies are selling uncooled infrared cameras that operate at video frame rates [10]. These cameras consist of a 320 × 240 array of pixels (microbolometers), each detecting infrared radiation via a radiation-sensitive material supported on a freestanding membrane. The membrane supports the

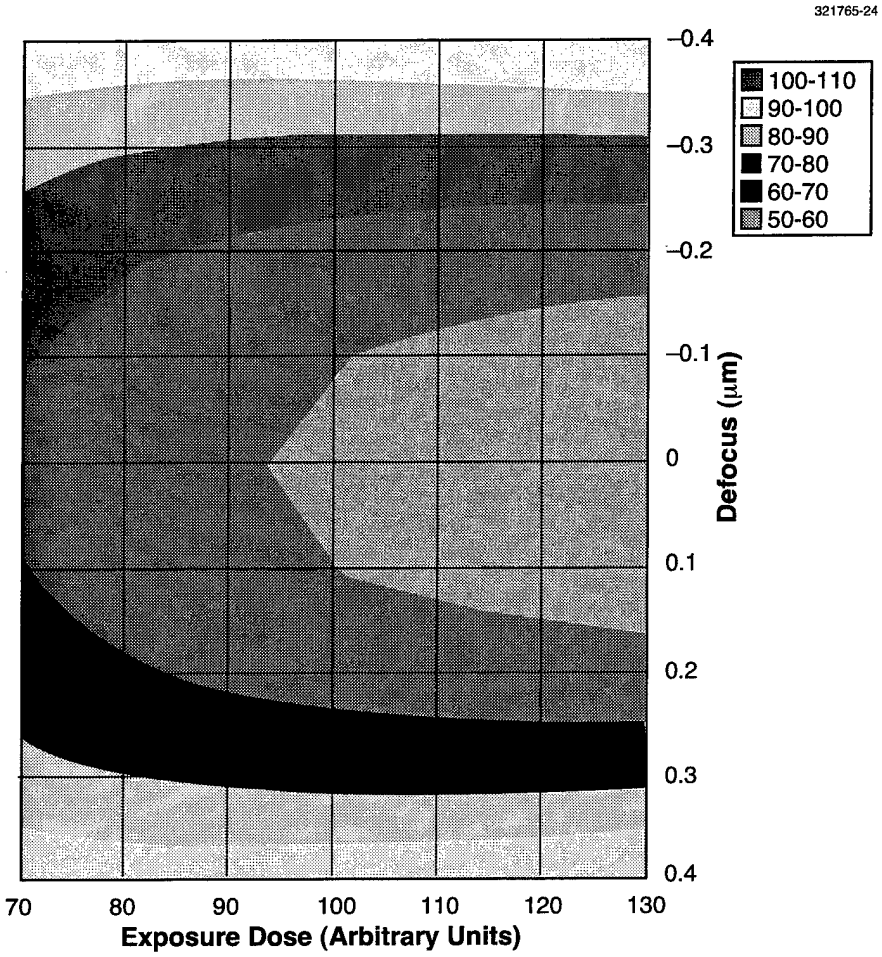


Figure 3-5. Calculated inverse image-log slope at all values of dose and focus for exposure conditions: λ = 193 nm, NA = 0.5, σ = 0.6, and nominal 175-nm linewidth (isolated). Contours represent lines of equal inverse image-log slope in nm.

high-TCR (temperature coefficient of resistance) material, provides thermal isolation from the substrate (control electronics), and must efficiently absorb the incoming radiation. In order to reduce the pixel size, and hence the cost and size of the camera, the dimensions of the microbridge membrane must shrink, while maintaining the necessary mechanical, spectral, and thermal properties, and the low cost of the membrane material.

The films were deposited from the vapor of liquid organosilicon precursors, shown in Figure 3-6, and oxygen-containing gases in a conventional 13.56-MHz rf-powered parallel-plate reactor. The rf power

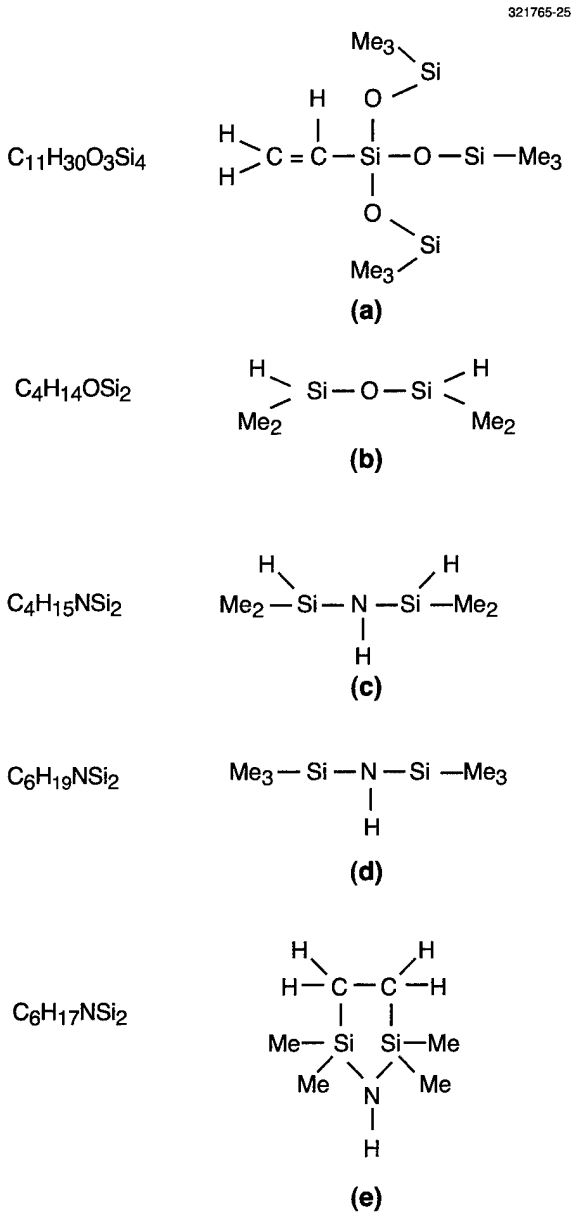


Figure 3-6. Plasma-enhanced chemical vapor deposition (PECVD) precursor materials.

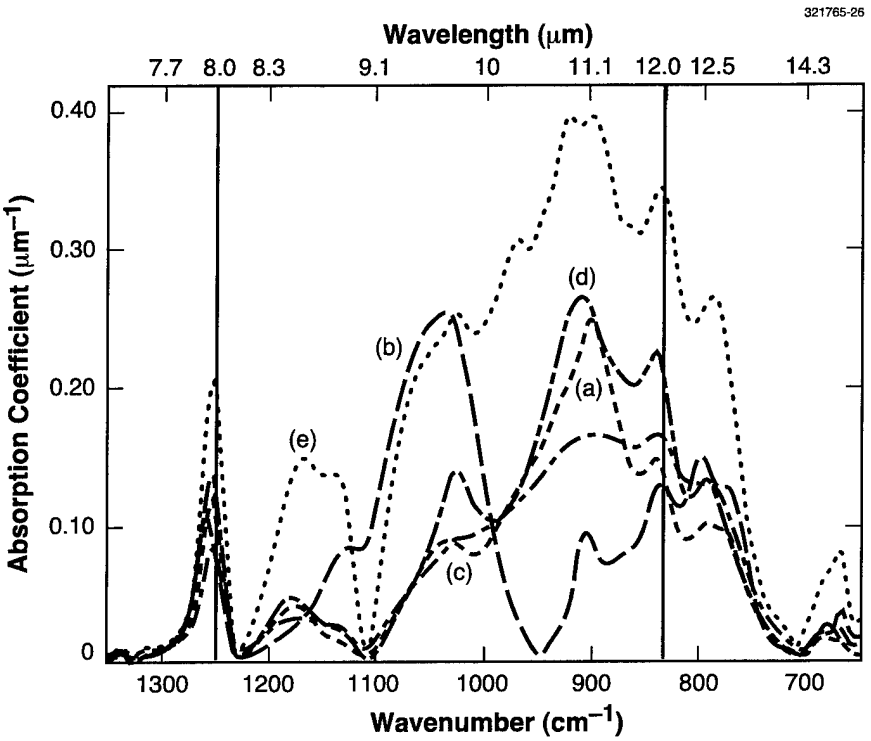


Figure 3-7. Normalized FTIR absorbance spectra for PECVD films from various silicon-containing precursors. The letters correspond to those in Figure 3-6, which describes the chemical structure for each different precursor.

was applied to the lower electrode, and it was varied from 50 to 400 W. Gases were introduced through a water-cooled shower head in the top electrode at flow rates from 1 to 200 sccm. Films were deposited at relatively high pressures (50-1000 mTorr) onto 4-in. wafers which were robotically loaded onto the bottom, temperature-controlled (powered) electrode.

Figure 3-7 shows the Fourier transform infrared (FTIR) absorption spectrum for a variety of compounds with strong vibrational spectra in this wavelength range. Figure 3-6 shows the chemical structure for each compound. In Figure 3-7 one can see that the precursor gases have a strong effect on the film absorption characteristics in the infrared. After screening several precursors with respect to ease of deposition, film uniformity, and resistance to buffered HF (BHF) solution, we focused our studies on films deposited from tetramethyldisiloxane (TMDS) and tetramethyldisilazane (TMDZ), having structures (b) and (c) in Figure 3-6, respectively. Figure 3-8 shows FTIR spectra for three different films. In this case we have supplemented the silicon-containing precursors with oxygen, in an attempt to enhance the absorption coefficient at ~1100 cm^{-1}, which is the signature of Si-O bonds. Indeed, the optical absorbance of TMDZ at ~10 μm increases dramatically with the addition of oxygen, partly at the expense of absorption at 900 cm^{-1}

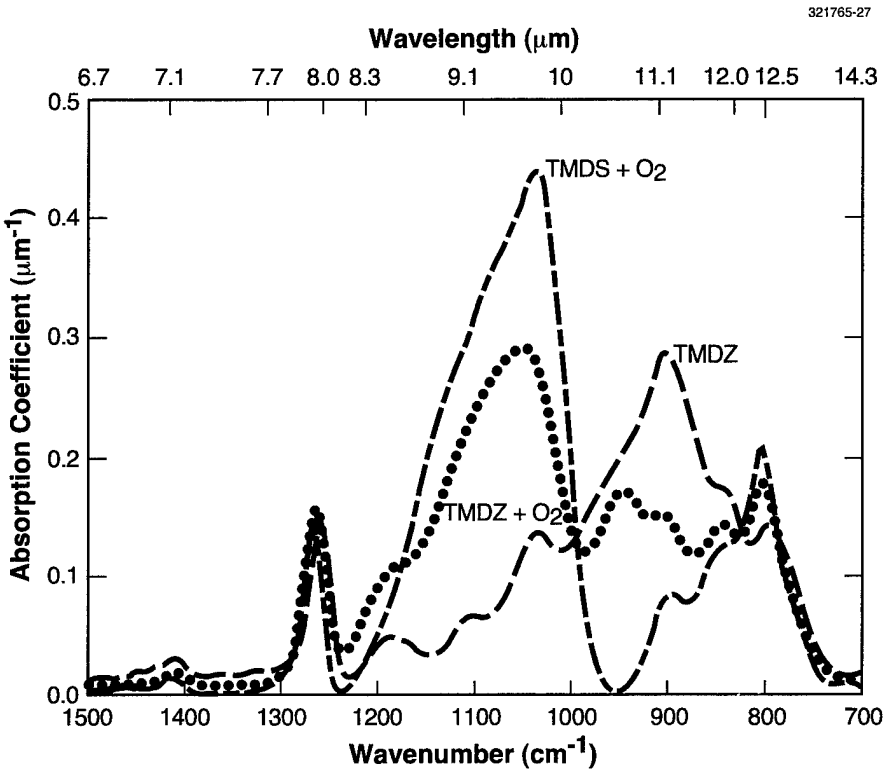


Figure 3-8. Fourier transform infrared (FTIR) absorbance spectra for films made from TMDZ, TMDZ + O_2, and TMDS + O_2. The addition of O_2 dramatically increases the absorption at ≈ 9.5 μm.

(Si-N bonds). Thus, the absorption of the films can be tailored by choosing the appropriate precursors, as required by the specific application. There may be a trade-off, however, between strong absorption over a narrow spectral range and reduced absorption over a broader width.

In general, the deposition rate is most strongly affected by the deposition pressure. Also, films deposited without the addition of oxygen are more polymeric in composition, and thus have no appreciable etch rate in BHF, while those deposited with oxygen etch more rapidly. Lastly, the hardness of the films, determined qualitatively by a scratch test, increases with rf power and decreases with increasing pressure. These trends are consistent with the plasma deposition dynamics, because in both cases the dc self-bias increases, thereby increasing the film density and hardness.

Films of varying thickness deposited under conditions that yielded oxide-like or polymer-like films were then evaluated for thermal conductivity. Figure 3-9 plots the thermal resistance as a function of thickness for four different films. In addition to the oxide-like and polymer-like TMDS-based PECVD films, silicon nitride and spin-coated polymethylmethacrylate (PMMA) are shown for comparative purposes.

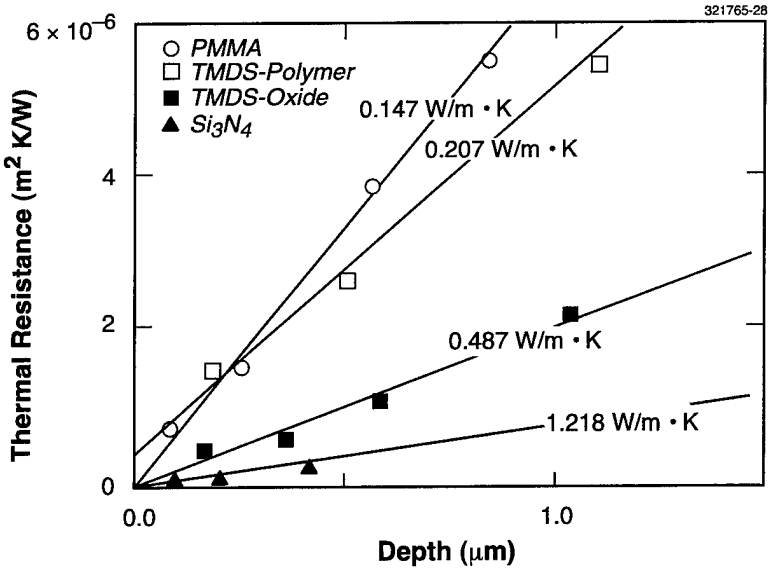


Figure 3-9. Measured thermal resistance as function of depth for four different films: sputtered silicon nitride, PMMA, polymer-like TMDS, and oxide-like TMDS. Lines show linear fits resulting in the values of thermal conductivity shown.

Because of its high tensile strength, silicon nitride has been the material of choice used in the formation of membranes for uncooled infrared detectors. The slope in Figure 3-9 for the silicon nitride yields a value for thermal conductivity k of 1.20 W/m K. This is close to the value reported using the 3ω technique [11], but much lower than the value of 5 W/m K listed for bulk silicon nitride [12]. The small negative intercept in Figure 3-10 is not yet fully explained, but is apparently an artifact of the thin-film deposition process. For calibration purposes, all the values of thermal conductivity in Figure 3-9 are referenced to a value of thermal conductivity for thermal oxide of 1.0 W/m K. PMMA was measured to have a thermal conductivity of 0.13 W/m K, almost an order of magnitude lower than that of silicon nitride. Note that the polymer-like TMDS films have a thermal conductivity of 0.21 W/m K, which is ~6 times less than that of silicon nitride, but still twice as large as that of a hydrocarbon polymer such as PMMA. For comparison, we note that the bulk thermal conductivity of a silicon-containing polymer, poly(dimethylsiloxane), is quite similar, 0.22 W/m K [13]. Also note that the PECVD oxide-like TMDS films are a factor of 2 higher in thermal conductivity than the polymer-like films (0.49 vs 0.21 W/m K).

In general, mechanical properties such as Young's modulus and Poisson's ratio are difficult to measure in thin films. We measured the intrinsic stress of films deposited from TMDS by measuring the bow of a 4-in. silicon wafer before and after deposition. Depending on deposition conditions, films 0.5 μm thick were deposited with less than 1×10^{10} dynes/cm^2 compressive stress. However, most of our mechanical evaluation was done by depositing films under different deposition conditions and of differing thicknesses

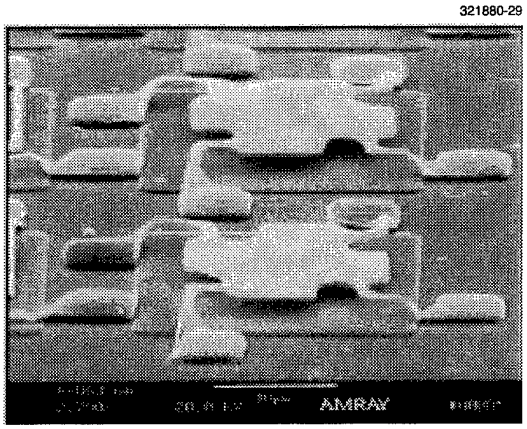


Figure 3-10. Scanning electron micrograph of four-legged freestanding membrane fabricated using TMDS films 0.9 μm in thickness.

and then fabricating freestanding membranes by the process described previously. Figure 3-10 shows a typical fabricated test structure. The membrane thickness is 0.9 μm and the width of the legs measures approximately 2.2 μm. The membranes shown in Figure 3-10 would have adequate mechanical strength for 60 × 60-μm (nominally 2 mil) pixels.

Although we have demonstrated a membrane whose thickness is uniform, an ideal microbolometer bridge material might be one in which the cross-sectional profile of the film is purposefully tailored during the deposition. This can be achieved by exploiting the custom in-situ chemical synthesis enabled by the PECVD process [14] and results in the ability to decouple the various thermal and mechanical properties by providing distinct PECVD film regions, each optimized for a given property.

M. W. Horn
R. B. Goodman
M. Rothschild

REFERENCES

1. D. E. Seeger, D. C. La Tulipe, Jr., R. R. Kunz, C. M. Garza, and M. A. Hanratty, *IBM J. Res. Dev.* **41**, 105 (1997).
2. M. W. Hibbs and R. R. Kunz, *Proc. SPIE* **2440**, 40 (1995).
3. S. C. Palmateer, R. R. Kunz, M. W. Horn, A. R. Forte, and M. Rothschild, *Proc. SPIE* **2438**, 455 (1995).

4. J. P. Holland, presented at the 44th Gaseous Electronic Conference, 1991 (unpublished); U.S. Patent No. 4,948,458 (1990).

5. J. Hutchinson, Y. Melaku, W. Nguyen, and S. Das, *Proc. SPIE* **2724**, 399 (1996).

6. S. W. Pang and M. W. Horn, *J. Vac. Sci. Technol. B* **8**, 1980 (1990).

7. M. W. Horn, S. W. Pang, and M. Rothschild, *J. Vac. Sci. Technol. B* **8**, 1493 (1990).

8. M. W. Horn, M. Rothschild, B. E. Maxwell, R. B. Goodman, and L. M. Eriksen, *Appl. Phys. Lett.* **68**, 179 (1996).

9. P. Finney, *Sensors* **13**, 36 (1996).

10. P. L. Marasca and E. L. Dereniak, *Proc. SPIE* **2020**, 363 (1993).

11. S.-M. Lee and D. G. Cahill, *J. Appl. Phys.* **81**, 2590 (1997).

12. Y. S. Touloukian and C. Y. Ho, eds., *Thermal Conductivity of Nonmetallic Solids*, Vol. 2 of *Thermophysical Properties of Matter* (IFI/Plenum, New York, 1970), p. 662.

13. J. F. Mark, ed., *Physical Properties of Polymers Handbook* (AIP Press, Woodbury, N.Y., 1996), Chap. 10, p. 111.

14. M. W. Horn, B. E. Maxwell, R. B. Goodman, R. R. Kunz, and L. M. Eriksen, *J. Vac. Sci. Technol. B* **14**, 4207 (1996).

4. HIGH SPEED ELECTRONICS

4.1 MICROWAVE MEASUREMENTS OF SiC VERTICAL FIELD-EFFECT TRANSISTORS

SiC-based vertical field-effect transistors (VFETs) have been designed, fabricated, and tested. The unique feature of the device is its submicrometer-periodicity U-groove grating structure which enables several potential performance advantages with respect to both planar FETs and vertical static induction transistors (SITs) for high-frequency high-power applications. Small-signal rf measurements have been obtained on VFETs fabricated on both 6H- and 4H-SiC substrates.

The preferred device configuration for high-voltage high-frequency power VFETs (and SITs as well) is the source-up version, that is, with the top ohmic contact serving as the source and the substrate ohmic contact as the drain. This is primarily due to the ease with which low-doped drift regions (for high voltage capability) can be formed below the level of the etched grooves (the gate region). In addition, the frequency capability of the source-up VFET is superior to its drain-up counterpart (provided the top ohmic contact is not severely compromised by either process or material limitations) owing to gate capacitance considerations.

Two-port small-signal S-parameter measurements were made on a number of source-up 6H-SiC VFETs from 0.1 to 18 GHz using a Hewlett-Packard 8510 network analyzer and cascade probes. Cascade probe calibration was performed off-chip; thus, all measured results include device parasitics. For the current device layout the top bridging contact forms a grounded contact for all presently configured on-wafer cascade probes. For source-up devices the bridging contact feeds the source pad, facilitating straightforward common-source rf measurements. Maximum stable gain, maximum available gain, and short-circuit current gain (h_{21}) can be calculated from the measured S-parameter data, and both the unity current gain frequency F_t and maximum frequency F_{max} can be determined from appropriate extrapolations to the unity gain frequency. Figure 4-1 displays h_{21} vs frequency for the best source-up 6H-SiC VFET. The F_t is 3 GHz; F_{max} (not shown) was less than 1 GHz for this device.

The relatively low F_t and rf gain for this first device can be easily explained. To facilitate current-voltage testing at various stages of fabrication, large gate shorting bars were incorporated into the initial design. These bars add considerable parasitic capacitance to the gate contact. Simulations suggest they reduce F_t by a factor of 2 compared to our standard test devices. Even more important is the very high source-series resistance apparent in these devices. The high source resistance comes from primarily two sources: high specific contact resistance due to lower than desired top ohmic region doping plus a nonoptimized ohmic contact process, and the very low mobility associated with the C-axis channel of 6H-SiC. It should be pointed out that our simulations suggest that transconductances 6–7 times higher than the measured devices should be achievable for 6H-SiC source-up devices with optimized source contacts, in spite of this low channel mobility.

Similar S-parameter measurements were made on a number of drain-up 4H-SiC VFETs. 4H-SiC is well known to have superior mobility compared to 6H-SiC (anywhere from 3–6 times higher) in the C-axis

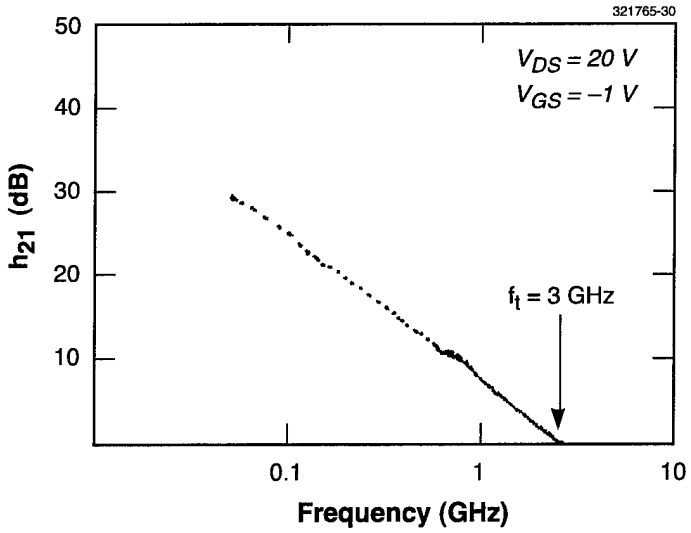


Figure 4-1. The h_{21} vs frequency data calculated from two-port S-parameter measurements on source-up 6H-SiC vertical field-effect transistor (VFET). The unity current gain frequency F_t (h_{21} at 0 dB) is 3 GHz.

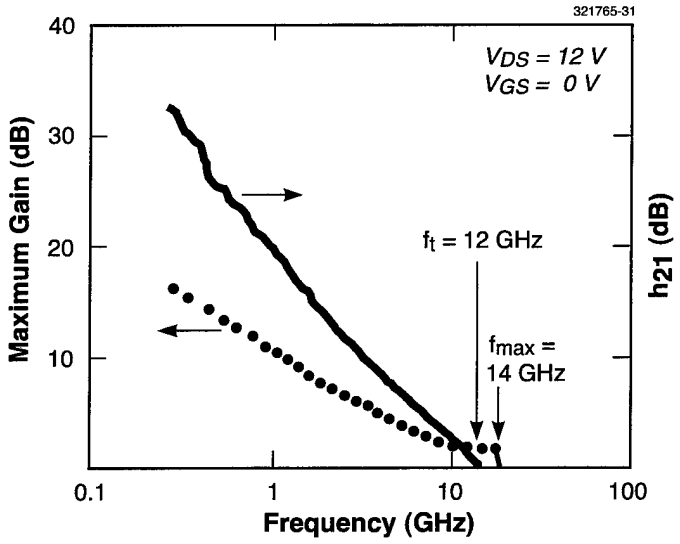


Figure 4-2. The h_{21} and maximum available gain vs frequency calculated from S-parameter measurements on drain-up 4H-SiC VFET. F_t and F_{max} are 12 and 14 GHz, respectively.

direction and thus is preferred for vertical devices in SiC. (6H-SiC was initially cheaper and more widely available than 4H-SiC.) It was determined early on that the 4H-SiC wafers obtained from Cree Research would not yield adequate and reliable top ohmic contacts necessary to produce good source-up devices, because of inadequate n^+ doping. It was therefore decided to fabricate drain-up VFETs using a forward-biased Schottky as the drain. Drain-up VFETs are more easily fabricated than source-up devices because the Schottky drain contact can be formed simultaneously to the Schottky gate contact at the groove bottoms. While less useful in real applications, drain-up devices can nevertheless serve as an indicator of potential rf performance until the development of the top ohmic contact necessary for source-up devices is optimized.

For drain-up devices the bridging contact is part of the drain; thus, common drain measurements are preferred. It should be noted that h_{21} for both common-source and common-drain modes is functionally equivalent and therefore yields the same F_t. The maximum stable gain and maximum available gain have somewhat different S-parameter expressions but nevertheless yield nearly the same $F_{\max}$ provided device parasitics are not excessive. Figure 4-2 shows h_{21}, maximum stable gain, and maximum available gain for our first drain-up 4H-SiC VFET vs frequency. F_t was measured to be 12 GHz with $F_{\max}$ near 14 GHz. This is particularly encouraging for the following reasons: (1) the devices have some unmodulated current and do not pinch off well, and thus the maximum gain is lower than it should be; (2) another device wafer of equivalent material, which subsequently broke before completion and testing, exhibited nearly twice the maximum gain of the measured wafer with good pinch-off behavior; and (3) this material is highly defective and considered to be less than optimal. Device F_t's in excess of 20 GHz seem realizable even for drain-up devices, with the added expectation that equivalent source-up devices should yield F_t's significantly higher.

D. D. Rathman
G. D. Johnson

5. MICROELECTRONICS

5.1 RESISTIVE-GATE CCD TECHNOLOGY

The standard fabrication technology for charge-coupled devices (CCDs) since the early 1970s has been the overlapping gate process based on polysilicon. Although this approach has worked well for devices with areas up to several square centimeters, there are applications in broad-area space surveillance and astronomy where devices having areas of tens of square centimeters are desired. Such devices demand the most stringent process conditions in order to avoid shorts between adjacent gates. We describe here a CCD structure called the resistive-gate CCD (RGCCD) that offers relief from the difficulties of the overlapping-gate approach and may lead to significant yield improvements for wafer-scale devices.

The conventional overlapping-gate CCD, depicted in Figure 5-1(a), is characterized by closely spaced gates fabricated in two or more layers of polysilicon. The gates overlap each other but are kept electrically isolated by a thin (typically 200–400 nm) layer of thermally grown SiO_2. For high yield the defect density of the SiO_2 must be kept low to prevent electrical shorts between gates. The RGCCD also dates back to the early years of CCDs [1] and is depicted in Figure 5-1(b). Here, the gates are all fabricated in a single layer of polysilicon in which highly doped regions are separated by undoped or lightly doped regions. An alternative to polysilicon has been reported in which a GaAs CCD was made using metal gates separated by cermet (Cr/SiO) resistive films [2]. The resistive areas ensure a uniform electric field distribution along the surface between the conductive polysilicon. The resistive-gate approach avoids gate overlaps which is one of the principal factors limiting yield. In addition, the interelectrode capacitance of this structure is much less than for the overlapping-gate approach, and this translates into lower power dissipation.

Another advantage of the resistive-gate device lies in the fact that it can be used to make relatively large pixels and thus move charge over long distances with few clock cycles. In some imaging applications the spatial resolution of the image is much coarser than the pixel dimensions of typical CCDs, and the CCD would therefore oversample the image. Increasing the pixel size to match the imaging requirements is not a practical alternative for pixel sizes more than about 30 μm because of the very weak horizontal drift fields under such long gates and the resulting long charge-transfer times. In the overlapping-gate CCD the drift fields are concentrated at the edges of the gates and are relatively weak toward the centers, and in this sense this structure is inefficient in its use of the clock voltages for propelling charge. In the RGCCD, however, the voltage is used to maintain uniform drift fields over a potentially large fraction of the pixel, and this translates into efficient charge transfer over large distances between gates. As an example, a typical minimum drift field in the CCD for the AXAF program [3] is about 1000 V/cm in a three-phase, 24-μm pixel. Such a field could be produced in an RGCCD with a 10-V bias across two gates separated by 100 μm, suggesting that a 300-μm, three-phase pixel is feasible.

We have fabricated a test imager and associated test structures on the mask set to explore RGCCD technology. The sheet resistance of the resistive gate is a critical parameter for the success of this approach for large-area devices. The lower limit on the sheet resistance is determined by the power dissipation in the

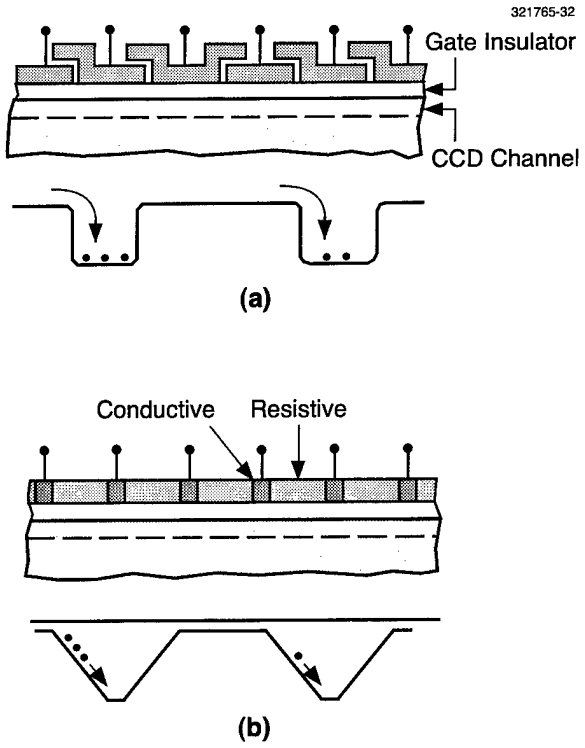


Figure 5-1. Comparison of (a) conventional overlapping-gate charge-coupled device (CCD) structure and (b) resistive-gate CCD.

resistive sheet, while the upper limit is set by the RC-time constant (resistance of the film and its capacitance to the substrate) and thus the maximum clocking speed. The range of acceptable sheet resistances turns out to be roughly 10^8–10^{10} Ω/square for various imager designs that we have examined.

Our preferred choice for the gate material is polysilicon doped by ion implantation. Prior work in fabricating highly resistive polysilicon films suggests that the resistivity can be more easily controlled with *p*-type than *n*-type polysilicon [4]. We have therefore chosen to dope the resistive portions of the gate with BF_2 at an energy of 35 keV. Figure 5-2 shows data on the sheet resistance vs temperature for a 50-nm polysilicon film implanted at a dose of 2×10^{12} cm^{-2}. The resistance has a temperature dependence which has been fitted to a curve of the form

$$\rho_s \propto T^{-2/3} \exp\left(E_a/kt\right) \quad , \tag{5.1}$$

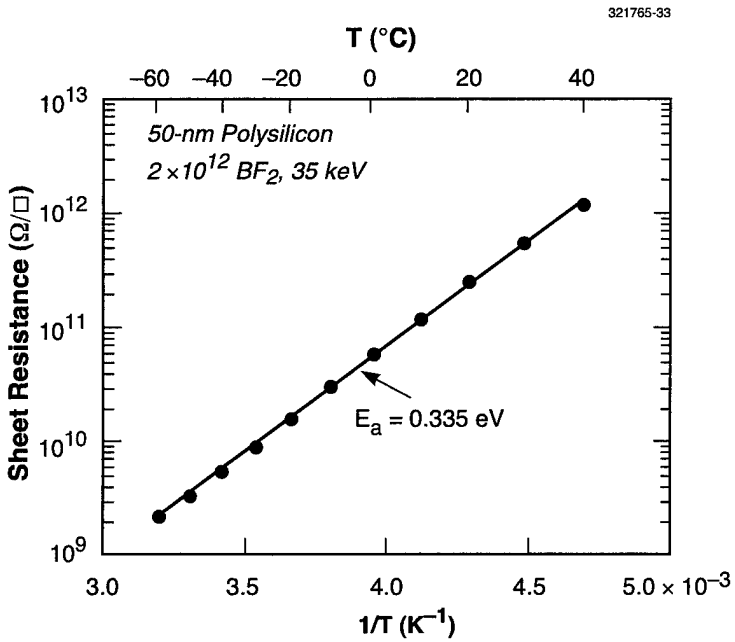


Figure 5-2. Measured sheet resistance of p-type polysilicon doped with ion implantation vs temperature.

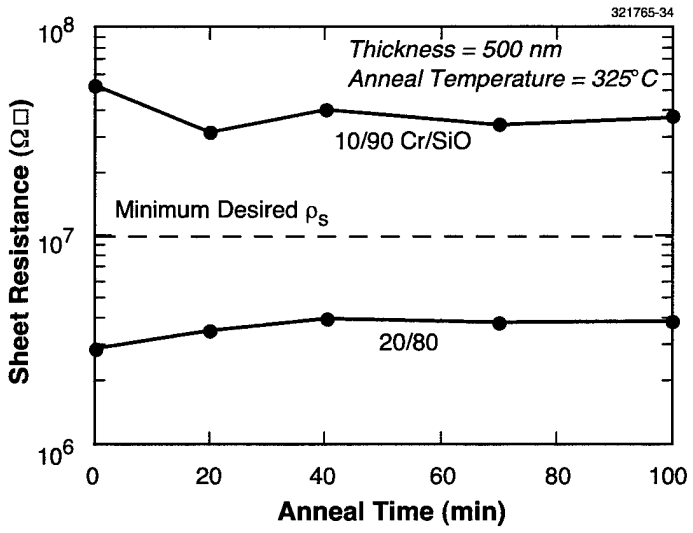


Figure 5-3. Measured sheet resistance of 500-nm-thick cermet films of two compositions as a function of anneal time.

where ρ_s is the sheet resistance, T the absolute temperature, and E_a the activation energy. The value of E_a = 0.335 eV is in agreement with previously reported results for this doping level [4]. The resistance of this film turns out to be too high to allow operation of the CCD serial register except near room temperature and above. However, we found at these temperatures that the serial register could not be clocked fast enough to prevent saturation of the device with dark current. Higher implant doses will be tried on the remaining wafers in the lot in order to adjust ρ_s downward.

The strong temperature dependence of ρ_s for lightly doped polysilicon is somewhat undesirable because it limits the operating temperature range of a device for optimum speed and power dissipation. We are exploring thin films of cermet (Cr/SiO) as an alternative resistive layer and expect this material to have a much lower temperature coefficient of resistivity. Films of 500-nm thickness and Cr/SiO percent compositions of 10/90 and 20/80 were evaporated on glass slides. Since the CCD process uses a deposited oxide over the resistive gate we annealed these films in air at the oxide deposition temperature and tracked the changes in resistivity. The results in Figure 5-3 show that ρ_s is relatively stable for anneal times well in excess of the oxide deposition time. In addition, the 10/90 composition is comfortably above the desired minimum sheet resistance, assuming a film thickness of 50 nm would have 10× higher ρ_s. One issue that needs to be resolved, however, is trace amounts of impurities such as Au and Fe in the cermet charge that are deleterious to silicon devices.

B. E. Burke
D. J. Young
C. C. Cook
J. A. Gregory
V. S. Dolat
D. M. O'Mara

REFERENCES

1. C.-K. Kim and E. H. Snow, *Appl. Phys. Lett.* **20**, 514 (1972).
2. J. A. Higgins, R. A. Milano, E. A. Sovero, and R. Sahai, *Proceedings of the GaAs IC Symposium* (IEEE, New York, 1982), p. 49.
3. B. E. Burke, J. A. Gregory, M. W. Bautz, G. Y. Prigozhin, S. R. Kissel, B. B. Kosicki, A. H. Loomis, and D. J. Young, *IEEE Trans. Electron Devices* **44**, 1633 (1997).
4. T. Kamins, *Polycrystalline Silicon for Integrated Circuit Applications* (Kluwer, Boston, 1988), p. 155.

6. ANALOG DEVICE TECHNOLOGY

6.1 TRANSMIT FILTERS FOR WIRELESS BASESTATIONS

A 3-pole filter for basestation transmit applications has been developed based on the vertical coupling of three stripline disk resonators, fabricated using high temperature superconductive (HTS) thin films. These resonators operate in the TM_{010} mode, where all the rf currents flow radially. This avoids the current crowding associated with the more conventional microstrip resonators, which severely limits the power handling of filters [1]. The use of a vertical architecture allows the use of films on 2-in. wafers for operation at frequencies near 2 GHz, allocated for the use in basestations for personal communication systems (PCS).

The 3-pole filter consists of three coupled circular stripline resonator structures. Each resonator is fabricated using two, 20-mil-thick, 2-in.-diam $LaAlO_3$ wafers having YBCO films deposited on both sides of the substrate by reactive coevaporation [2]. Two circular discs, approximately 39 mm in diameter, are patterned on the facing side of the wafers, the other two sides functioning as ground planes. The YBCO is patterned using positive photoresist and ion beam etching. Each ground plane is patterned with a small disc in the center, separated by a YBCO free annulus from the rest of the ground plane. Gold contacts are formed by evaporation and lift-off on this center disc, and on two annular areas, one around the gap and another on the outer edge of the ground plane. After the photolithography the substrate is annealed in oxygen at 500°C. Films of Au/Ti are sputter deposited on both sides of the wafer and around the edge, using a metal mask. They provide contact between the ground planes of the two wafers. The two wafers are bonded together using polymethylmethacrylate (PMMA). A film approximately 2 μm thick of PMMA is spun on each wafer. The gold contact around the edges is wiped clean. The substrates are heated to 160°C for 20 min in an oven to remove any solvents. The wafers are then bonded by squeezing them together using a vacuum jig and heating them up to 140°C. The bond that is formed withstands further processing and has minimal effect on the Q of the resonator in the operating range 50–70 K. The alignment between the structures on the two wafers is done mechanically by referencing all the patterns to the edge of the wafers. The resonance frequency of a number of similarly fabricated devices had a maximum variation of 1 MHz for a resonance frequency near 1.95 GHz. The coupling to the resonators is done capacitively by two 1-mm-diam discs soldered to the center conductor of two 0.141-in. coaxial cables placed on each side of the resonators' package. The coupling can be adjusted easily by varying the spacing between the copper discs and the center discs patterned on the two ground planes.

Table 6-1 summarizes the results of our measurements. The Q between 50 and 70 K is almost entirely defined by losses in the substrates [3]. The measured power handling is hundreds of times that of 3-mm-wide microstrip resonators made with similar films [1].

The center frequency of each resonator can be adjusted up to 4 MHz, by opening a series of 1-mm circular or square holes in one of the ground planes in the region corresponding to the edge of the disc resonator. These holes had minimum effect on the resonator Q but reduced the maximum circulating power by

TABLE 6-1
Unloaded Q and Power Handling for a Stripline Disk Resonator

Temperature (K)	Unloaded Q	Power Handling (MW)
13	1.46×10^6	2.5
20	1.41×10^6	2.6
40	4.6×10^5	2.9
50	1.25×10^5	1.85
60	7.6×10^4	1.48
70	9.65×10^4	0.72

up to a factor of 5, for the maximum frequency shift. (For this test we removed four equidistant arcs, 1 mm wide and 1 cm long, in one ground plane.) However, for the maximum tuning required by the 1-MHz observed resonance frequency variation, the maximum circulating power is decreased by a factor of only 1.9.

Figure 6-1 shows an exploded view of the 3-pole filter. It consists of three stripline resonators separated by gold-plated Ti spacers. Each spacer has a 1-cm hole in its center and also holes corresponding to the tuning structures on the ground plane of one of the adjacent wafers, the other wafer having been left intact. In the center hole a donut-shaped piece of $LaAlO_3$ is used to position a springy, gold-plated, copper-beryllium bellows between the central circle in the two adjacent ground planes, providing the necessary coupling between adjacent resonators. The input/output structures consist of a copper cup, soldered to the outer conductor of the input/output coaxial cable and a bellows soldered to the center conductor. The three wafers and two separators are squeezed together by a bed of springs while the two coaxial cables and copper cups are forced against the wafers by two springs. The copper cups make contact with the gold annuli patterned on the ground planes of the resonators. The whole structure can be disassembled in a few minutes, and successive measurements of the reassembled filter's frequency response are indistinguishable.

The procedure used for synthesizing the filter is the following: The equivalent circuit elements are determined by a conventional synthesis technique [4] and verified using circuit analysis software. The size of each resonator and the coupling structure are then determined using a commercially available two-dimensional finite element differential equation solver. The whole structure is then further analyzed using three-dimensional microwave analysis software.

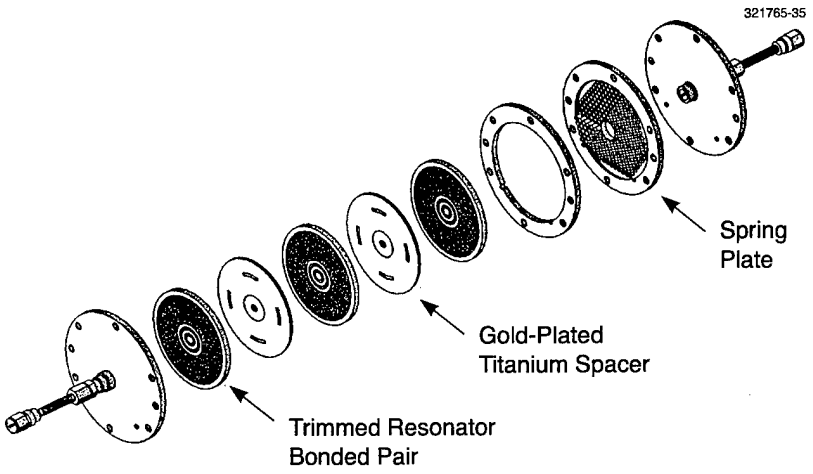


Figure 6-1. Exploded view of 3-pole filter.

The filter was originally synthesized as a Chebyshev filter with a ripple of 0.1 dB and a bandwidth of 0.75%. The measured response of the original filter had a 1.5-dB valley in the passband. Using measurements that isolate the different coupling structures, we determined that the input and output coupling structures had been synthesized correctly. However, the interresonator coupling had not. The original simulation did not account for air gaps between the bellows, $LaAlO_3$ donut, and ground planes. We also realized that by adjusting the resonance frequency of the middle resonator we would produce a filter with a slightly wider bandwidth and a uniform ripple of 0.5 dB. This adjustment was beyond what could be achieved by opening holes in the ground plane as discussed previously. A new center resonator was fabricated. The measured and calculated frequency response and return loss of this corrected filter are shown in Figure 6-2 at 50 K and for an input signal of 1 mW. Also shown in Figure 6-2 is the frequency response at 72 W, the maximum power presently available to us at the input of the filter. The measured frequency response was very close to what we predicted and no tuning was required. For these measurements we used a He-filled can with the filters mounted on a cold finger thermally anchored to the cold head of the cryocooler. The measurements for Figure 6-2 were made using a single sweep mode. The insertion loss of the filter at 1 mW or 72 W is less than 0.1 dB, the accuracy of our measurement. If we use a cw tone, the thermometer mounted on the filter registers an increase of temperature of 0.2 K, commensurate with a dissipation of about 1 W in the filter. However, this is the same for signals in band or out of band and can be attributed to power dissipated in the cables connected to the filter. Figure 6-3 shows the frequency response of the filter plotted over a wider frequency range. Besides the desired passband, a secondary structure is evident at frequencies around 2.17 GHz. This corresponds to the coupling of the "pillbox" modes of the resonators at these frequencies and will be discussed further later.

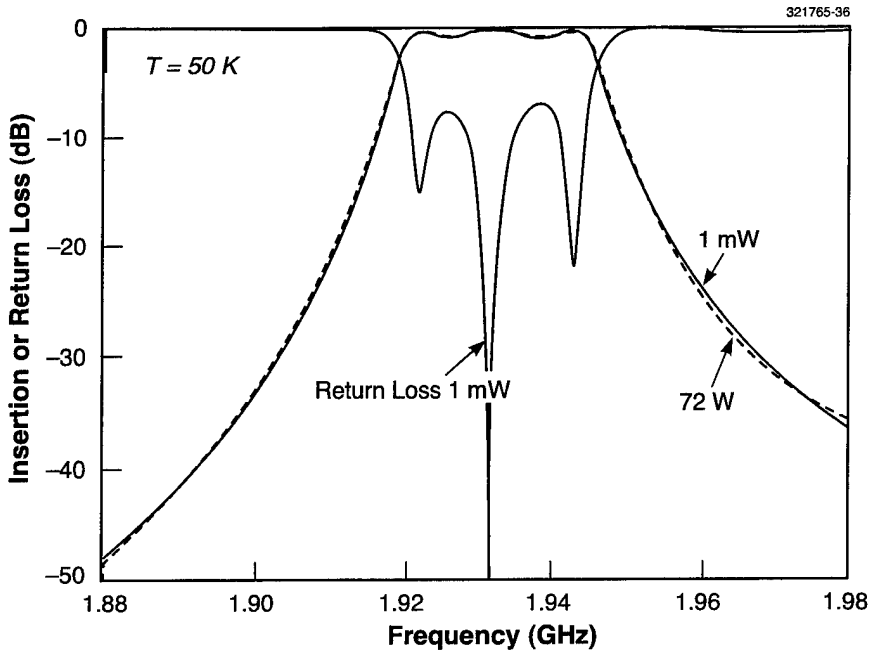


Figure 6-2. Frequency response of 3-pole filter for frequencies near passband.

We have attempted to measure the intermodulation products for two in-band tones. Our present testing system requires the two input tones to be matched within 0.5 dB, and that limits our setup to 20-W input to each channel. Up to this limit the intermodulation products are indistinguishable from the ones produced by the system without the filter. Our measurements indicate that the third-order intermodulation product is at least 104 dB below each input tone for an input level of 43 dBm for each of the two tones.

The choice of coaxial filter structure was strongly influenced by the operation frequency and available film size. Our goal of building a 9-pole transmit filter for PCS applications, using a planar layout, would require $LaAlO_3$ wafers with diameters larger than 5 in. This vertical structure, however, offers a number of advantages over the more conventional planar one. First, it is very compact, with a 9-pole filter occupying a volume less than 35 cm^3, including the packaging. Second, since resonators and resonator pairs can be tested, it is easy to verify and adjust the accuracy of the design without having to build the filter. Because of the cylindrical symmetry, only the TM_{0n0} modes of the resonators are excited. We looked for and did not find any of the TM_{mn0} modes with $m \neq 0$. The extra peaks in the frequency response of the filter in Figure 6-3 are caused by the coupling of the cylindrically symmetric pillbox modes for the three resonators. This is clearly seen in the finite element analysis, which is particularly effective in identifying the eigenmodes for the symmetric structure. The mode of these extraneous resonators presently limits the out-of-band rejection of the filter to 50 dBc near the band edge and 28 dBc near 2.2 GHz. It can be moved

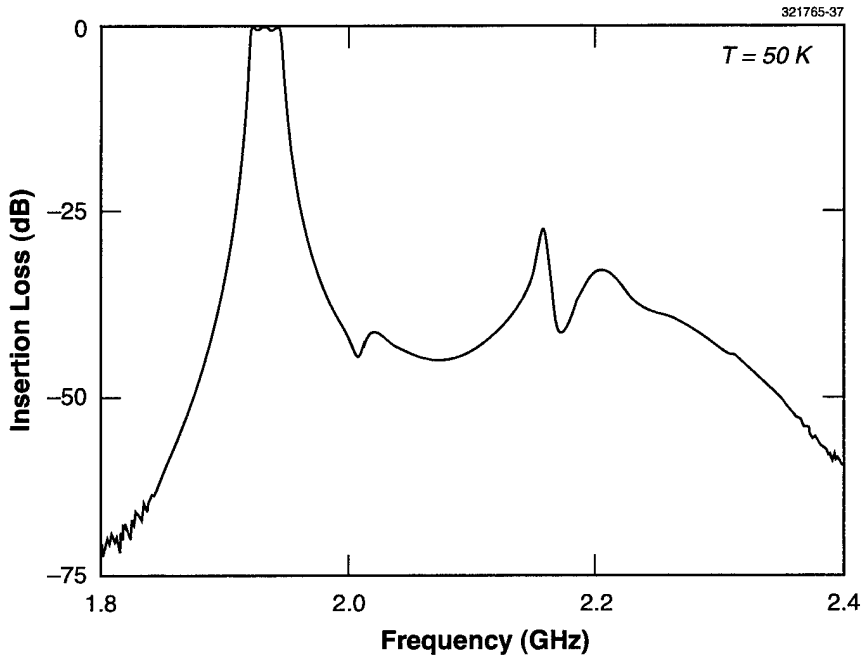


Figure 6-3. Wideband frequency response of same filter as for Figure 6-2. The extraneous peaks near 2.2 GHz are caused by coupling of the pillbox mode of the three resonators.

to higher frequencies by reducing the size of the wafers. Alternatively, the Q of the undesirable resonance can be substantially reduced by substituting part of the YBCO ground plane, outside the area of the circular resonator, by a lossier, normal metal conductor. This has been accomplished for individual resonators with no impact on the Q of the main resonance, but we have not yet implemented filters incorporating these changes. Simulation based on the resonator results shows that the spurious response can be reduced below 90 dBc. The measured out-of-band suppression at frequencies lower than the passband is better than 90 dBc.

The calculated losses [5] due to the power dissipated in the resonators for a measured Q of 100,000 at 50 K is 0.02 dB. To these losses we must add the dissipation in the bellows contact assembly. For 70-W input, the input and output rf currents are 1.2 A, while the current in the interresonator bellows near the band edge is 2.8 A. An estimation of the total resistance for gold-plated bellows is 0.002 Ω, resulting in a total dissipated power of less than 40 mW. This is compatible with the measured insertion loss of less than 0.1 dB. This calculation ignores the contact resistance between the bellows and the gold contact on the films. Our measurements place a maximum value of 0.1 Ω for this contact resistance.

The measured circulating power for the resonators can be extrapolated to the power handling of the filters [5]. The maximum circulating power occurs for frequencies near the band edge. If we use the measured circulating power for the resonators at 50 K, we find that the filter should handle more than 5 kW.

Our measurements of intermodulation products and of the power handling are consistent with these estimations. Similar calculations show that a 9-pole 0.75% bandwidth filter could handle power above 1 kW. It is likely that other factors will limit the filter performance at these high powers.

A. C. Anderson
Z. Ma*
P. M. Mankiewich*
T. Kaplan*
H. Wu*
P. A. Polakos*
A. Barfknecht*

REFERENCES

1. Solid State Research Report, Lincoln Laboratory, MIT, 1997:1, p. 41.
2. V. Matijasevic, Z. Lu, T. Kaplan, and C. Huang, *Proceedings of EUCAS,* H. Rogalla and D. H. A. Blank, eds., *Institute of Physics Conference Series*, No. 158, 1997, p. 189.
3. C. Zuccaro, I. Ghosh, K. Urban, N. Klein, S. Pennan, and N. M. Alford, *IEEE Trans. Appl. Supercond.* **7**, 3715 (1998).
4. G. L. Matthaei, L. Young, and E. M. T. Jones, *Microwave Filters, Impedance-Matching Networks and Coupling Structures* (McGraw-Hill, New York, 1964).
5. M. A. Hein, C. Bauer, W. Diete, S. Hensen, T. Kaiser, G. Müller, and H. Piel, *J. Supercond.* **10**, 109 (1997).

*Author not at Lincoln Laboratory.

7. ADVANCED SILICON TECHNOLOGY

7.1 IMPLEMENTATION STUDY FOR THE ANOMALY CODING COMPRESSION ALGORITHM

A study has been undertaken at MIT Lincoln Laboratory of possible implementations in hardware of a novel algorithm, the anomaly coding (AC) algorithm [1], for compressing data from infrared atmospheric sensors aboard a NASA earth observation satellite. Four such implementations are examined here. The first three are based on commercial chips and therefore have the advantage of low cost and a shorter design cycle. The fourth includes an application-specific integrated circuit (ASIC) that could be built in Lincoln Laboratory's fully depleted 0.25-μm silicon-on-insulator (SOI) CMOS process. It has the following potential advantages: (1) Our estimates indicate that the ASIC's total power consumption would be lower than for commercial chips by as much as 2 orders of magnitude. As we will describe, the ASIC-based implementation would also include a commercial microprocessor, but that microprocessor could be of much lower power than the commercial chips in the other three implementations. (2) There may be greater resistance to radiation in the ASIC case because of the inherent radiation resistance of the SOI process. The commercial chips are not manufactured in radiation-hard versions at present.

The primary goal of the satellite-borne measurement system is to map the temperature of the atmosphere as a function of altitude and global position. This is to be accomplished by recording the intensity of infrared radiation received from the atmosphere at 2400 spectral bands between 3.8 and 15.4 μm. A compressed version of this data will be transmitted to the ground, where it will be used in an atmospheric model to obtain a best-fit temperature profile. As the satellite orbits, it will take readings from successive sets of 90 points in the atmosphere along a line parallel to the earth's surface and perpendicular to the plane of the orbit. The set of readings for all 90 points takes 2 s and is called a scan. The combined readings of the 2400 sensors at a single point in the scan is called a sounding. There will not be enough downlink bandwidth to transmit all the sensor data, so a data compression algorithm, described in the next section, must be used. The algorithm employs a priori knowledge of the statistics of the received atmospheric signal and of the noise (contributed mostly by the sensors).

First, we present a high-level description of the AC algorithm. The goal of the algorithm is to achieve good (typically better than 10 to 1) compression of remote sensing data by explicitly attempting to discard *only* white noise in the data. The AC algorithm relies on a technique called noise-adjusted principal components (NAPC) [2]. This is an extension of the classical principal component analysis of multivariate statistics: Given a set of, say, spectral data, classical principal component analysis computes a linear change of coordinates in such a way that as much of the variation as possible in the original data is now concentrated in a small number of spectral components. By retaining only these so-called principal components, one achieves data compression with a set of components which is smaller in number than the original set, but represents an acceptably large fraction of the variation of the original data. (The effectiveness of the technique relies on the existence of linear dependencies in the original data; the more such dependencies, the smaller the size of the resulting component set.) When working with noisy data, though, one faces a

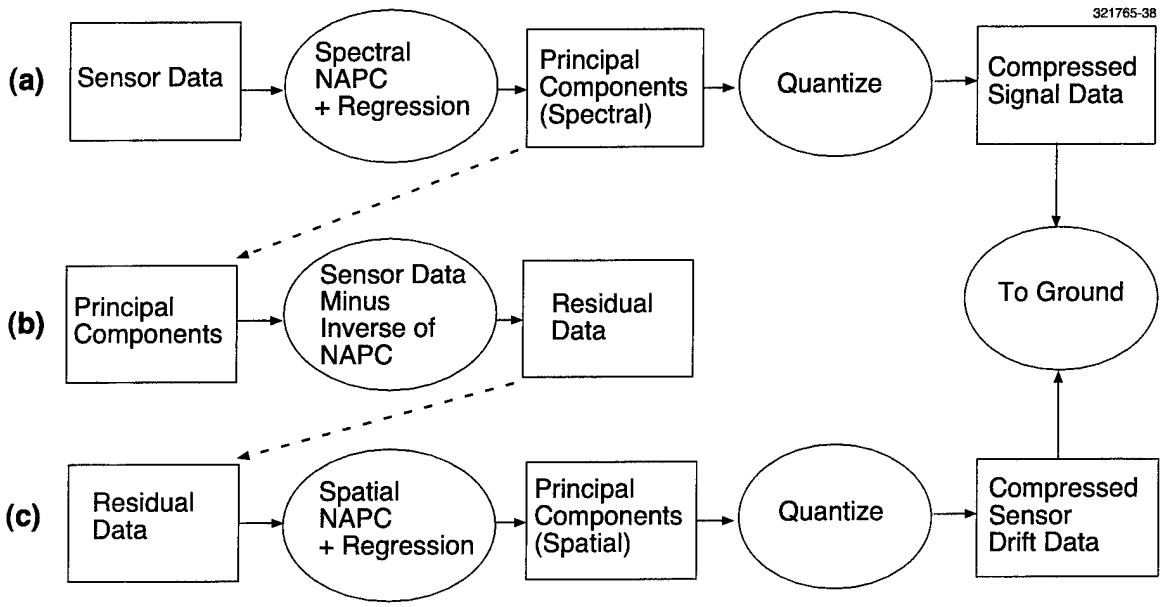


Figure 7-1. Block diagram of anomaly coding algorithm.

problem: Even if the principal components represent most of the variation in the original noisy signal, they may have a smaller (perhaps much smaller) signal-to-noise ratio (SNR) than the original data, in which case the real signal variation captured by the principal components may be unacceptably low. The NAPC technique addresses this problem.

The NAPC technique modifies the classical method of principal component analysis by applying a preliminary coordinate change that ensures that, in the new coordinate units, the noise amplitude in each spectral component has the value 1. (In general, it is possible to isolate noise in this way if signal and noise are known to be statistically independent, and if one has reliable a priori estimates of mean and covariance for both signal and noise. In our case, signal and noise mean values and covariance matrices have been computed from simulated data, and are assumed to be reasonable approximations for the requirements of the NAPC computation.) Next, coordinates are changed again in the manner of principal component analysis, but in such a way that the value of noise amplitude is not affected. This means that, in the resulting set of spectral components, if one chooses a component with high amplitude, then automatically one is choosing a component with high SNR. Thus, one is free to choose a set of principal components, knowing that this set will not only capture a high fraction of the variation of the original data but will also have a high SNR. (As we've noted, one obtains a small number of principal components, that is, a high degree of data compression, when there is sufficient linear dependence in the original data.) This is the general sense of the NAPC technique.

The AC algorithm employs NAPC compression across the spectral data of each sounding. This process is illustrated in line (a) of Figure 7-1. The process begins with the step denoted spectral NAPC + regression in Figure 7-1, which represents the NAPC transformation itself, composed with a linear regression to separate signal from noise. Computationally, this step is a large matrix multiplication. ("Large," in our case, approximately amounts to the multiplication of a 2400-element vector by a 200 × 2400 matrix; there are approximately 2400 spectral elements in each sounding, and experience with prior data shows that approximately 200 principal components are sufficient to yield a result exhibiting "negligible" signal degradation: "Linear statistical temperature retrievals from simulated clear radiances without anomalies were degraded less than 0.008 K rms at all levels when anomaly coding was applied to the data" [1].) Following this spectral NAPC/linear regression step, we have a scaled quantization of the principal component output of the coordinate change, denoted quantize in line (a) of Figure 7-1. By "scaled," we mean that bits are apportioned to each spectral component in proportion to the contribution that component makes to the variation of the data set.

The AC algorithm continues with the preparation of input data for a spatial NAPC computation, as indicated in line (b) of Figure 7-1. The single computational step in line (b) is denoted sensor data minus the inverse of NAPC. In this step, we first multiply the principal component vector obtained in line (a) by the inverse of line (a)'s NAPC transformation, yielding an estimate of geophysical signal in the original sensor data. (Note that this is the same data-recovery operation that will be performed on the ground.) This restored signal is then subtracted from the original sensor data to give us a vector denoted residual data, which is an estimate of the noise in the original data. As in line (a), the computation is dominated by a large matrix multiplication (in our case, this approximately amounts to the multiplication of a 200-element vector by a 2400 × 200 matrix). The algorithm maintains one scan's worth of residual data for the spatial NAPC, the actual calculation of which is done in step (c) of Figure 7-1.

The purpose of the spatial NAPC stage of the algorithm is to take into account $1/f$ drift in sensor noise. Whereas the spectral NAPC calculation was performed across the spectrum, separately for each sounding, the spatial calculation is performed across all soundings of a scan (i.e., across 90 data points), separately for each spectral frequency. This calculation is performed in line (c) of Figure 7-1, in the single step denoted spatial NAPC + regression. The purpose here is analogous to line (a); there, we compressed sensor data and extracted signal information from it. This signal information is ultimately transmitted to the ground. In line (c), we compress the residual, that is, the noise in the original sensor data, and extract sensor white noise from it. This compressed sensor noise will ultimately be transmitted to the ground and combined with the reconstituted signal so that a filtered version of the sensor data with reduced white noise is obtained. (Recall that the spectral NAPC process required signal and noise to be statistically independent, and that we have a priori estimates of their mean and covariance. Similarly, the spatial NAPC process requires that sensor noise and white noise be statistically independent, and that we have a priori estimates of their mean and covariance as well.) Because the calculation can't be performed until data from all soundings of a particular scan are present, the partial computation performed at each sounding is actually a part of the spatial NAPC calculation from the previous scan.

The burden of computation represented in line (c) of Figure 7-1 is not significant compared to the matrix multiplications of lines (a) and (b), and will not subsequently be dealt with in this report. Similarly,

the scaled quantization of lines (a) and (c) is computationally insignificant compared with the matrix multiplications, and will not subsequently be dealt with. Finally, at the beginning and end of each scan, data calibration is performed which, since it too is not computationally significant compared with the matrix multiplications, will not subsequently be dealt with.

We have just seen that the computational burden in this algorithm is borne essentially by two matrix multiplications, namely, the matrix multiplications represented in lines (a) and (b) of Figure 7-1. The computational precision required in these matrix multiplications is as follows [3]: 16 bits for the sensor data input in line (a); 16 bits for the elements of the matrix in line (a); 21 bits for the principal component output in line (a), which is also the principal component input in line (b); 17 bits for the elements of the matrix in line (b); and 24 bits for the residual data output in line (b).

Note that each numerical multiplication that occurs in the matrix multiplication in line (b) has operands of 21 and 17 bits. In the ensuing discussion of possible hardware implementations of this algorithm, one of the architectures we consider is the Texas Instruments (TI) TMX320C6201 digital signal processing (DSP) chip. Multiplication on this chip is limited to 16-bit operands. So, in the case of the TI DSP chip, we will make two accommodations. First, we will employ 16 rather than 17 bits to represent the matrix elements in line (b) of Figure 7-1. In so doing, we will incur a 10% increase in distortion [3]. (Distortion is a quadratic measure of the difference between the ideal and extracted geophysical signal.) Second, we will think of the input vector in line (b) of Figure 7-1 as being broken up into two vectors, the first having 16-bit entries and the second having 5-bit entries. Each of these two vectors must be separately multiplied by the matrix in line (b), and then the two results combined via a (computationally insignificant) shift and accumulate. So, in the case of the TI DSP architecture, the computational burden actually consists of three, rather than two, matrix multiplications, with an increase in distortion of about 10% over the other architectures we will discuss. In the case of these other architectures, the computational burden still consists of only two matrix multiplications.

As the primary goal of this study is to examine hardware configurations that can perform the AC algorithm at the required rate, four such configurations are examined in the following sections. The first three are based on commercial chips and therefore have the advantage of low cost and a shorter design cycle. The fourth includes an application-specific integrated circuit (ASIC) that could be built in Lincoln Laboratory's fully depleted 0.25-μm SOI CMOS process. Its potential advantages are lower total power and the greater resistance to radiation inherent in the SOI process. No attempt has been made to choose among the four alternatives.

In the following paragraphs, we address the suitability of implementing the AC algorithm using the TI TMX320C6201 fixed-point DSP. We address the performance of this DSP with regard to computational and I/O burden. The TI TMX320C6201 fixed-point DSP contains eight functional units and a 32K by 32-bit addressable memory, with a highest-performance rating of 200 MHz. In programming this DSP, full eight-fold parallel processing is not usually attained, because each type of instruction can actually be executed only by a proper subset of the eight functional units.

The AC algorithm consists primarily of matrix multiplication, so we first determine the cost of performing matrix multiplication on this DSP. In the 22 ms following the acquisition of data from one sounding to the next, we will perform a spatial NAPC computation, the front end of a spectral NAPC computation, and the back end of a spectral NAPC computation using data from the previous scan. In terms of assessing computational cost, we can think of the spectral NAPC computation as amounting to multiplication of a 2400-element vector by a 200 × 2400 matrix, where each vector and matrix element is represented by 16 bits, as described previously. We can think of the back end of the spectral NAPC computation as amounting to multiplication of a 200-element vector by a 2400 × 200 matrix, where each matrix element is represented by 16 bits and each vector element is represented by 21 bits. Finally, we can regard the spatial NAPC computation as being (relatively) computationally insignificant.

As noted previously, this DSP chip permits at most 16-bit inputs to multiplication. Since the vector elements in the back end of the spectral NAPC computation are 21-bit numbers, we will think of that vector as being broken up into two vectors, the first having 16-bit entries and the second having 5-bit entries. Each vector must separately be multiplied by the appropriate matrix, and then the two results combined via a (computationally insignificant) shift and accumulate.

This all amounts to 200 inner products of vectors of size 2400, followed by 2400 inner products of vectors of size 200, done twice (once for a vector with 16-bit entries and once for a vector with 5-bit entries), representing a total of three matrix multiplications. To assess the computational cost of these three matrix multiplications, we begin by assessing the cost of an inner product: The operations that shoulder the burden in the computation of an inner product are add, load, and store, each of which can (with some limitations) be performed simultaneously in one clock cycle on this DSP; and multiply, which can (with some limitations) be performed simultaneously with add, load, and store in two clock cycles. With these constraints the inner product of two 8-element vectors (each element being a 16-bit fixed point number) can be computed in 12 clock cycles using a 32-instruction subroutine, as shown in Figure 7-2. (We are assuming that a series of these products is being computed, so that there is a savings of two clock cycles due to pipelining, as indicated in Figure 7-2. The variables A0–15 and B0–15 in Figure 7-2 denote 32 user-programmable registers.)

To compute the inner product of two N-element vectors, one can break the problem up into a series of inner products of 8-element vectors, and then accumulate the partial products. The overhead for this accumulation is minimal, so that, just as it requires 1.5 × 8 clock cycles to find the inner product of two 8-element vectors, it takes about $1.5 \times N$ clock cycles to find the inner product of two N-element vectors. Applying this estimate to the inner products required in our three matrix multiplications yields 2.16×10^6 clock cycles. At 180 MHz, with some padding for overhead, the computations require 14 ms.

Having estimated the computational cost per sounding, we now estimate the I/O cost. We assume that the two matrices are held in off-chip memory. Given the sizes of the matrices (200 × 2400 and 2400 × 200), we require 1 megaword of 16-bit or 32-bit memory. SGRAM or SDRAM from Micron Technology satisfies these requirements. These memories have peak cycle times of 10 ns; furthermore, this DSP chip

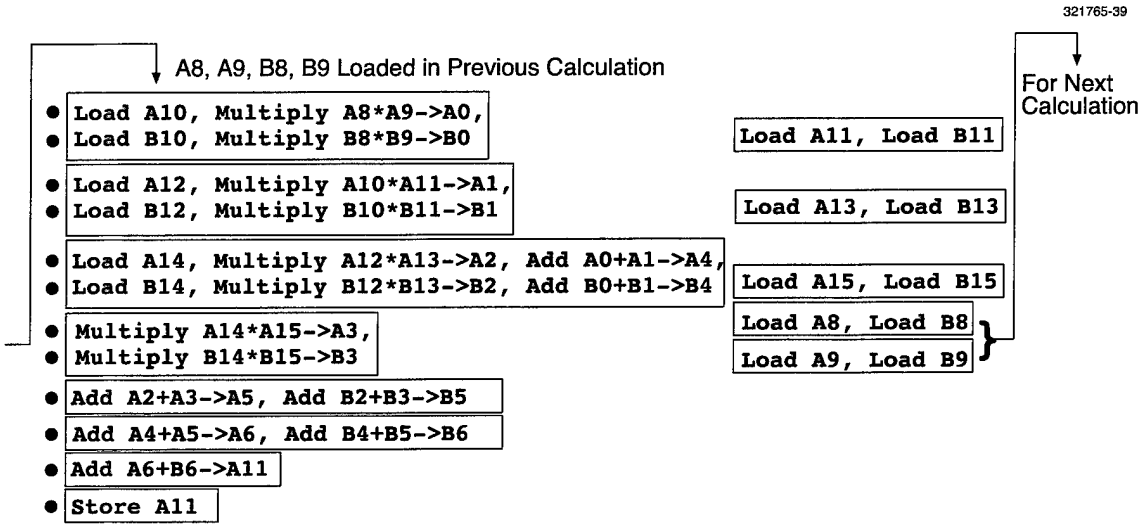


Figure 7-2. Inner product of two 8-element vectors.

provides "glueless" interfaces to such memories. The I/O burden consists primarily of moving the two matrices (in stages) from the SDRAM to the on-chip 32K memory. (Note that the algorithm uses one of these matrices to multiply by two different vectors, one with 16-bit elements and one with 5-bit elements; this accounts for our three matrix products.) This amounts to about 10^6 reads per sounding. But at one read per 10 ns, the total I/O cost is 10 ms.

Under our assumptions, computation plus I/O require 24 ms in the worst-case scenario, which is that there is no significant way to parallelize computation and I/O. Given that the time between soundings is 22 ms, we conclude that a system based on this DSP chip would require a scheme that is more computationally or I/O efficient than what has been described here. That there are such schemes will become evident below; the I/O-efficient scheme described there could be implemented in a DSP-based environment as well.

We now discuss implementing the AC algorithm using the Motorola DSP96002 general purpose floating-point processor. The computational and I/O requirements are the same as in the discussion of the TI DSP, except that we drop the restriction of 16-bit operands. We wish to first estimate the computational cost per sounding. In their documentation, Motorola describes a sample matrix multiplication program for this DSP. By using this program, multiplication of two $N \times N$ matrices requires about $2 \times N^3$ clock cycles. This program uses floating-point arithmetic. A conservative estimate based on Motorola documentation is that with so-called integer mode operations in place of floating-point operations, performance roughly doubles. Thus, by using integer arithmetic, multiplication of two $N \times N$ matrices requires about N^3 clock cycles. This chip can multiply 32-bit numbers, so there is no need to break the second matrix-vector multiplication into two parts. Now, as noted earlier, the computational burden of the AC algorithm for this archi-

tecture amounts to about 2400 × 200 multiplies and adds for each of two matrix computations. This is about the same number of adds and multiplies as occur in the product of two 80 × 80 matrices, done twice. According to the Motorola estimates, this computation consumes about 80^3 clock cycles for each of the two computations, or a total of 2×80^3 clock cycles. At 60 MHz, this DSP's top-rated speed, this is about 17 ms.

The I/O cost is calculated as above. In this case, given that the computational cost is 17 ms, and considering that the time between soundings is 22 ms, it is required that there be a more computationally efficient, or a more I/O-efficient, scheme than what is described here. That there are such schemes will become evident later; the I/O-efficient scheme described could be implemented in a DSP-based environment as well.

In addressing the suitability of implementing the AC algorithm using commercial CPUs, one processor type is investigated: the Motorola PowerPC family. We address the performance of these CPUs with regard to computational and I/O burden. The generic member of this CPU family allows two arithmetic instructions per clock cycle, with 32-bit integers. Referring to our computation estimate for the TI DSP, we see that our calculation was built around a routine to compute the inner product of two 8-element vectors, as shown in Figure 7-2. This routine has 32 instructions; so, as a conservative estimate, we assume that the equivalent routine in this case is simply a linearized version of that routine. Thus, 16 cycles are required to perform the basic computation. Reasoning as above, we see that, whereas in the case of the TI DSP it took $1.5 \times N$ clock cycles to compute the inner product of two N-element vectors, it takes $2 \times N$ clock cycles in the case of these PowerPC CPUs. Applying this estimate to the inner products required in our two matrix multiplications yields 1.92×10^6 clock cycles. At 180 MHz, with some padding for overhead, the computations require 12 ms. This clock speed makes sense for a 0.35-μm design rule PowerPC 603e, which is at the low end in terms of power consumption (4.0-W typical, 5.0-W maximum power consumption at 200 MHz). A faster alternative is the 0.29-μm design rule PowerPC 603e (4.0-W typical, 6.0-W maximum power consumption at 300 MHz). At 300 MHz, we estimate the computational cost at 8 ms.

The I/O cost may be estimated in the same way as the estimate for the TI DSP. Given our 22-ms window between soundings, we see that a scheme which is more computationally or I/O efficient would probably be necessary in the 200-MHz case. That there are such I/O-efficient schemes will become evident in the discussion below; the I/O-efficient scheme described there could be implemented in a commercial CPU-based environment as well.

One task of this study was to examine the suitability of using Lincoln Laboratory's 0.25-μm fully depleted SOI CMOS process to help achieve a compact, low-power implementation of the AC algorithm. A test chip with some signal-processing circuits has been made with this process and successfully tested at clock rates exceeding 1 GHz with a 2-V power supply. The inherent resistance of SOI to latchup caused by radiation could be an advantage in earth orbit. However, this report describes elsewhere a commercial DSP and a commercial microprocessor, either of which is capable of the necessary computation and data transfer rates. These devices are programmable and have built-in interfaces to the synchronous DRAM storage chips that would be needed for storing the large matrices needed in the AC algorithm. If low cost, short

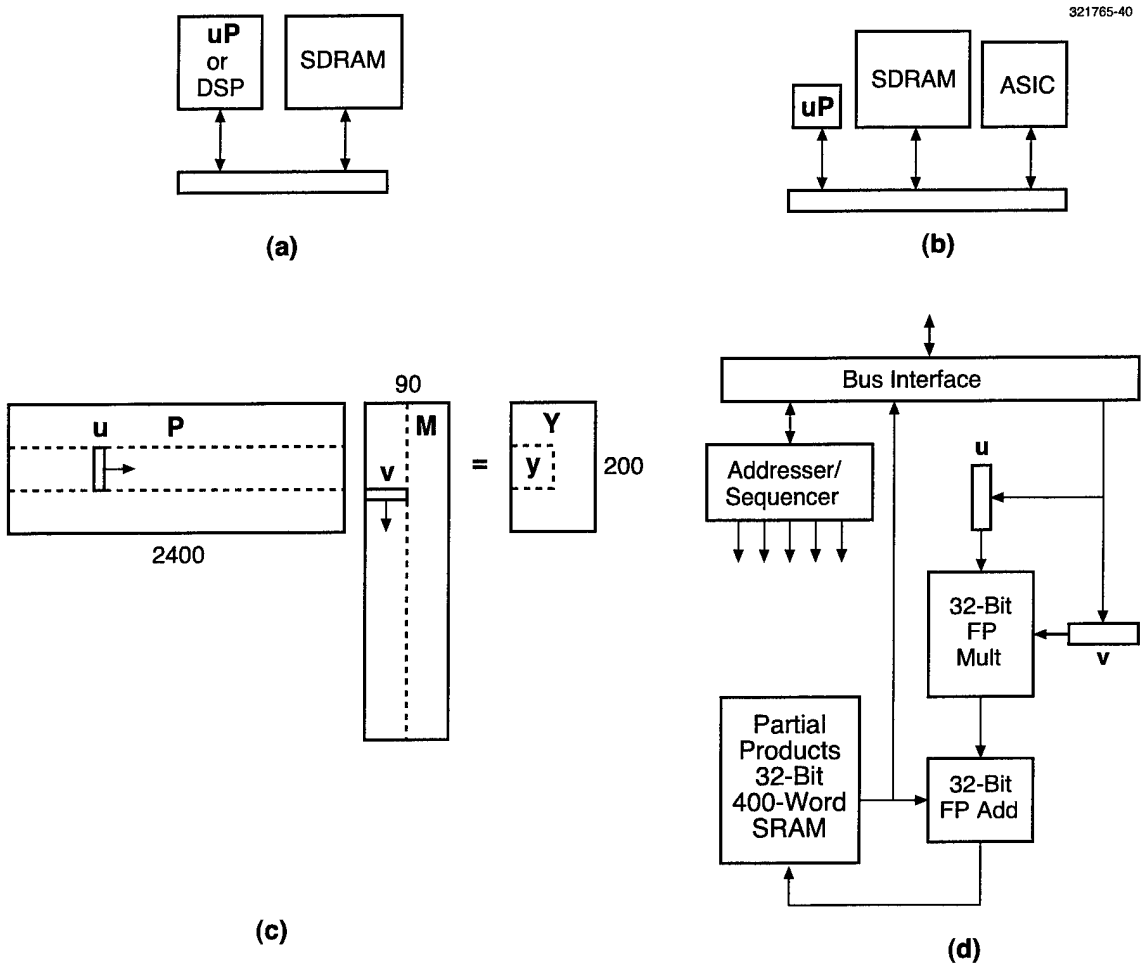


Figure 7-3. Hardware configuration with matrix multiplier application-specific integrated circuit (ASIC). DSP, digital signal processing; FP, floating point.

development time, or minimum risk are dominant considerations, then either of them would be preferable to a solution based on an a Lincoln-built SOI CMOS ASIC. However, if low power is most important, then the configuration shown in Figure 7-3 might merit consideration.

Figures 7-3(a),(b) compare the two hardware configurations using commercial chips only with the one about to be described, which uses a Lincoln-built ASIC as a matrix multiplication coprocessor. In Figure 7-3(b) the microprocessor is shown symbolically smaller, because the dominant portion of the calculation is the multiplication of large matrices, which will be performed by the ASIC. In Figure 7-3(a) a top-of-the-line microprocessor or DSP was needed to complete the calculations in time. In Figure 7-3(b) a much less capable, lower-power microprocessor could be used. Maybe the parts of the AC algorithm that

can't be done by matrix multiplication will represent a small enough load that they can be done in the main satellite instrumentation computer, in which case no extra microprocessor would be needed.

Figure 7-3(c) shows a scheme for partitioning the calculation of the matrix product to save on the loading of operands, applicable to any of the processor options. For example, the first large step in the processing of one full scan of data (90 soundings) is to multiply a 2400 × 90-element matrix **M** of measurements by a 200 × 2400-element fixed matrix **P**. This is the dominant operation in row (a) of Figure 7-1. In that analysis it was assumed that **P** was read from SDRAM for *each* sounding. This paragraph describes an approach that strongly decreases the total number of accesses to SDRAM. The matrix **M** represents not one sounding (a vector of 2400 values) but an entire scan of 90 soundings. Instead of operating on the first sounding as soon as it arrives, it is necessary to delay until several, in this case 20, soundings have arrived, each with 2400 spectral readings. Then the 20 columns of **M** spanned by the small row vector **v** may be multiplied by the 20 rows of **P** spanned by the small column vector **u**. The ASIC computes a 20 × 20 matrix of partial products, $\mathbf{y} = \mathbf{u} \cdot \mathbf{v}$, and then accumulates those partial products as **u** moves to the right and **v** moves down. When the accumulation is complete, that 20 × 20-element section of the product is stored into the SDRAM. Note that the computation of the entire product, $\mathbf{Y} = \mathbf{P} \cdot \mathbf{M}$, requires the loading of **P** from SDRAM not 90 times but only 5 times, once for each of the 20-wide vertical strips into which **M** can be partitioned. (The last strip needs to be padded with zeros, either in SDRAM or by the sequencer of the ASIC.) However, the measurement data needs to be loaded not just once, but 10 times, once for each of the 20-high horizontal strips into which **P** can be partitioned. The total number of loads from SDRAM is still reduced from $200 \times 2400 \times 90 + 2400 \times 90 \times 1 = 43.4 \times 10^6$ to $200 \times 2400 \times 5 + 2400 \times 90 \times 10 = 4.56 \times 10^6$, a factor of 9.5 reduction..

As described in the earlier schemes, the ASIC would have to do one multiply and one add every 10 ns, so the clock rate of the ASIC would be 100 MHz. Floating-point arithmetic was judged to be preferable to integer arithmetic, both because the shorter word length needed would actually result in a lower transistor count and because it would be easier to maintain the required precision throughout the several steps of the algorithm. Earlier designs in the SOI CMOS process had 10-bit integer adders that were designed to work at 1 GHz, so a 32-bit floating-point adder, properly pipelined, could easily be made to run at one tenth the speed. A 16-kbit SRAM chip is currently being designed to be clocked at nearly 2 GHz. The ASIC would need a 400 × 32 = 12 800-bit SRAM operating at 100 MHz, which should be easy to make.

An estimate of the power required by the floating-point portion of the ASIC can be made in a crude manner by counting the expected number of transistors and assuming that all their gates switch at half the clock speed, that is, 50 MHz. A reasonable average gate width is about 4 μm, which gives a gate capacitance of about 4 fF. Assume there is an equal amount of parasitic capacitance. Then the average power needed per transistor is $(1/2)CV^2f = 1/2 \times 8 \text{ fF} \times (1.5 \text{ V})^2 \times 50 \text{ MHz} = 450 \text{ nW}$, assuming a 1.5-V supply.

A rough estimate based on 25 transistors per 1-bit add-carry circuit suggests that the multiplier will have 7200 transistors and the adder 2000. Adding a little extra, the floating-point section should have about 10 000 transistors, whose power would be 4.5 mW.

Although the SRAM would have 12 800 × 6 = 76 800 transistors, only a small fraction would be switching at any time, so the SRAM power will be small compared to the floating-point power. Both of

them are small compared to the I/O power, which will be dominated by the driving of the addresses to the SDRAM. An earlier calculation showed that there would be 4.55×10^6 reads of SDRAM during a 2-s scan time for one of the two approximately equal large matrix multiplications that dominate the algorithm. Therefore, there would be about 10^7 reads of SDRAM every 2 s. Assume that the address lines each present a 50-pF load and that they toggle at every new address, that is, they charge up at a 2.5-MHz rate. About 24 bits would be needed to address the matrices, so the total addressing power would be $24 \times (1/2)$ 50 pF $\times$ $(3\ V)^2 \times 2.5$ MHz = 13.5 mW, assuming a 3-V swing on the memory bus.

By allowing a factor of 2 for other power dissipation, the ASIC should dissipate about 36 mW. The faster commercial processor chips dissipate several watts, so there is a potential for significant power savings with the ASIC, even if it has to be used with a weak microprocessor separate from the satellite's main processor.

This study has examined four different potential configurations of hardware, each of which is capable of executing the AC algorithm. Three employed commercial chips only, while the fourth included an ASIC custom built in the Lincoln Laboratory fully depleted 0.25-μm SOI CMOS process. Advantages and disadvantages of each approach were offered, but no recommendation of a preferred approach was made. Such a choice would have to be made in the context of the full satellite instrumentation system, something beyond the scope of this study.

Power requirements for each approach are summarized in Figure 7-1. The Lincoln ASIC does only matrix multiplications and must be used with a microprocessor to execute the compression algorithm. However, it could be a much less capable (i.e., lower power) microprocessor than those in Table 7-1.

TABLE 7-1
Summary of Processor Choices*

Processor	Power Dissipation
TI C6201 0.25 μm	5–6-W typical, 7-W maximum at 200 MHz
TI C6201 0.18 μm	1.8–2.2-W typical, 3-W maximum at 200 MHz
Motorola 96002	1.75-W typical at 60 MHz
PowerPC 603e 0.35 μm	4-W typical, 5-W maximum at 200 MHz
PowerPC 603e 0.29 μm	4-W typical, 6-W maximum at 300 MHz
Lincoln SOI CMOS ASIC	30–40-mW estimated at 100 MHz
*Ceramic 32 x 32-mm packages in all cases, except Lincoln ASIC.	

None of the commercial processors is sold in a radiation-hard version, and the radiation hardness of the commercial parts was not available. The Lincoln ASIC offers some promise of radiation hardness, because it is an SOI part, but no test data are available for its process either.

Before committing to a system based on the Lincoln ASIC, it might be advisable, for purposes of logic verification in hardware, to build a version of the ASIC using commercial gate arrays.

R. Berger
R. Frankel

REFERENCES

1. C. R. Cabrera-Mercader and D. H. Staelin, private communication.
2. J. B. Lee, A. S. Woodyatt, and M. Berman, *IEEE Trans. Geosci. Remote Sens.* **28**, 295 (1990).
3. C. R. Cabrera-Mercader, private communication.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (*Leave blank*)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	15 August 1998	Quarterly Technical Report, 1 May–31 July 1998

4. TITLE AND SUBTITLE

Solid State Research

5. FUNDING NUMBERS

C — F19628-95-C-0002

6. AUTHOR(S)

David C. Shaver

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Lincoln Laboratory, MIT
244 Wood Street
Lexington, MA 02420-9108

8. PERFORMING ORGANIZATION REPORT NUMBER

1998:3

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

HQ Air Force Materiel Command
AFMC/STSC
Wright-Patterson AFB, OH 45433-5001

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

ESC-TR-97-145

11. SUPPLEMENTARY NOTES

None

12a. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for public release; distribution is unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT (*Maximum 200 words*)

This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 May–31 July 1998. The topics covered are Quantum Electronics, Electro-optical Materials and Devices, Submicrometer Technology, High Speed Electronics, Microelectronics, Analog Device Technology, and Advanced Silicon Technology. Funding is provided by several DoD organizations — including the Air Force, Army, BMDO, DARPA, Navy, NSA, and OSD — and also by the DOE, NASA, and NIST.

14. SUBJECT TERMS

quantum electronics	high-speed electronics	lasers	Vertical field-effect transistors
electro-optical devices	microelectronics	epitaxial growth	charge-coupled devices
materials research	analog device technology	microlens alignment	transmit filters
submicrometer technology	advanced silicon technology	microelectromechanical systems	

15. NUMBER OF PAGES
93

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Same as Report	Same as Report	Same as Report